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Single-pulse avalanche mode operation of 10-kV/10-A SiC MOSFET

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ABSTRACT

The high-voltage silicon carbide MOSFET is a state-of-the-art solution for increasing power density and efficiency in power electronics; nonetheless, a full-scope of failure modes during extreme operating condition has not been established. Past efforts evaluated short-circuit capability of 10-kV silicon carbide MOSFET, however, in this manuscript, the single-pulse avalanche mode operation of a research-grade 10-kV/10-A silicon carbide MOSFET is explored for the first time. A decoupled unclamped inductive circuit was selected for evaluation, and avalanche energy was increased until catastrophic failure occurred. The maximum tolerable avalanche energy was measured to be 2.84 J corresponding to an energy density of 8.8 $J \cdot cm^{-2}$. This result was compared with 1.2-kV silicon carbide MOSFETs to evaluate device robustness. Post failure analysis included: estimation of junction temperature, scanning electron microscopy, and focused ion beam cut. Peak junction temperature of 1010 °C was estimated using a thermal RC model and measurement results suggested gate degradation as the primary mechanism responsible for device destruction. Microscopy of the device validated gate failure which occurred at, or beneath, the gate metallization. A narrow cavity with-in the failure region was discovered during failure analysis and is hypothesized to have protruded the epitaxial region of the semiconductor.

1. Introduction

Successful fabrication of the ultra-high voltage Silicon Carbide (SiC) MOSFET represents a significant breakthrough in SiC technology which possesses the potential to greatly evolve the field of power electronics. Inherent material properties of SiC, compared to its Silicon counterpart, have led to power semiconductor devices with increased blocking voltages, switching-frequency, and ambient operating temperature [1–8]. The superior material properties of SiC MOSFET make it suitable for a wide-variety of power electronic applications while also offering increases in system efficiency and power density [9–15]. As demand continues to grow for SiC devices, a more in-depth understanding of device reliability during extreme operating conditions must be established for widespread acceptance of the technology to occur [16–17]. The safe-operating-area (SOA) of a device provides a base-line understanding of device limitations, however in certain applications, operation beyond the SOA may occur during transient operation [18–22]. As a result, the short-circuit capability and avalanche energy tolerance are often considered as metrics of device robustness during transient operation. In both cases, high-power dissipation with-in the device under test (DUT) leads to increased electro-thermal stresses but the physical operation between each mode differs significantly. Most notably, during short circuit operation, the device is operating in the forward regime, however, during avalanche mode operation the device is operating in the blocking regime at voltages exceeding the rated capability [23–25].

Commercialization of SiC MOSFETs rated below 2 kV has occurred, where-as research grade devices have achieved blocking voltages up to 15 kV [26]. The commercial availability of devices with blocking voltages below 2 kV has led to an in-depth understanding of device robustness; in [27–29], the short-circuit limits were established, and in [30–33], the avalanche mode robustness was evaluated. Such empirical analysis is required to develop a fundamental understanding of device performance outside the designed SOA. As a result of limited availability, research grade high-voltage (≥ 10 kV) SiC MOSFETs have not been studied in such detail. In [18], the short-circuit capability of a 10-kV/10-A SiC MOSFET was presented; however, the avalanche energy capability and corresponding failure mechanisms have not been presented.

In this work, the single-pulse avalanche energy tolerance of a 10-kV/10-A SiC MOSFET, manufactured by Wolfspeed, is analyzed. Avalanche mode operation is induced to determine device robustness during extreme operating conditions. To establish robustness, the 10-kV device is compared with previously measured 1.2-kV SiC MOSFETs [33]. Additionally, a thermal analysis is performed to estimate junction temperature during device evaluation. Due to the limited nature of device dimensions, a Cauer model was realized and optimized based on calculated values of the junction thermal time constant. A decoupled unclamped inductive switching (UIS) circuit was used to allow for post-failure scanning electron microscopy (SEM) of the failure site occurring at the gate metallization. SEM of the device, in-conjunction with focused ion beam (FIB) cut, yielded evidence of melting and a

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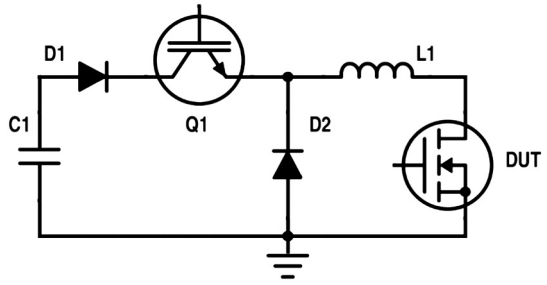

Fig. 1. Simplified UIS circuit schematic [33].

narrow cavity located beneath the gate bonding wire. Microscopy images of the failure site and measurement of the gate current during evaluation are utilized to hypothesize the failure mechanism leading to catastrophic failure.

2. Avalanche mode operation

Avalanche mode operation of the 10-kV SiC MOSFET was analyzed at 22 °C using a decoupled UIS circuit; the simplified circuit schematic is shown in Fig. 1 [33]. Q1 and D2 must be sufficiently rated for the maximum desired avalanche current and charging voltage of C1; in this case, Q1 (IXBT42N170) and D2 (DH60-16A) are rated for 1700 V/80 A and 1600 V/60 A respectively. The load inductor, L1, was air-core wound using litz-wire and measured to be 1.42 mH. During testing, the drain-to-source voltage, V_{DS}, was measured using a Northstar PVM-1 passive probe, and the drain current, I_D, was measured using a Stangenes pulse current transformer.

An example single-pulse avalanche waveform is shown in Fig. 2; the avalanche time duration is labeled t_{AV} and represents the integration boundary for energy calculations. V_{DS} and I_D are shown in the upper plot, whereas the calculated power dissipation, V_{DS} and I_D product, and resulting avalanche energy are shown in the lower plot. Results of Fig. 2 represent the maximum tolerable avalanche conditions, in-which, catastrophic device failure occurred upon further increasing avalanche

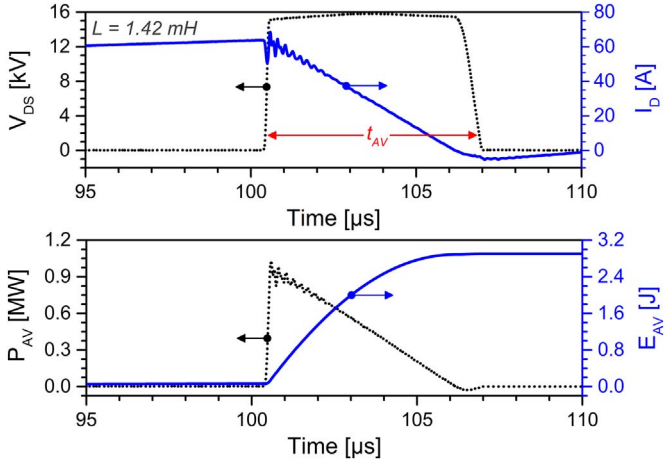

Fig. 2. Measured V_{DS} and I_D during avalanche mode operation (top); calculated device power dissipation and avalanche energy (bottom). The avalanche time duration is labeled in the upper graph and utilized to determine avalanche energy. Results represent final data-point prior to catastrophic device failure.

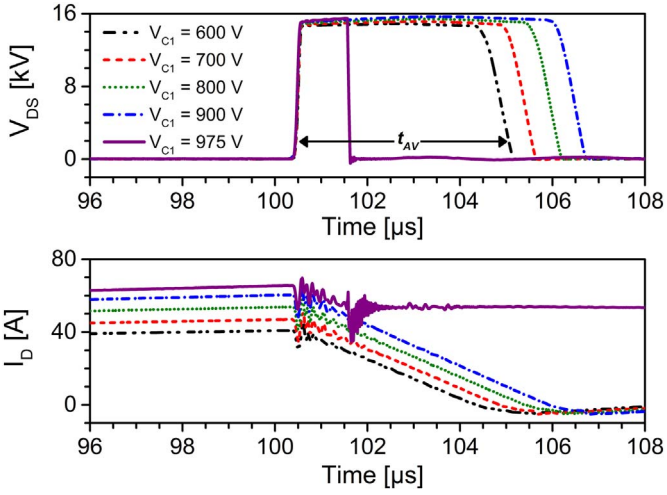

Fig. 3. Progression of measurement to failure; failure waveforms are shown with a solid line. V_{C1} represents the capacitor charging voltage for C1 in Fig. 1. Measured values of V_{DS} are shown in the top plot, and measured values of I_D are shown in the lower plot. The avalanche time duration is shown for V_{C1} = 600 V.

current. A more detailed methodology can be found in [33].

3. Avalanche energy tolerance

Evaluation of device robustness during avalanche mode operation was determined using a fixed inductor charging time of 100 µs, and the capacitor voltage, C1 in Fig. 1., was ramped in 25 V increments up to catastrophic device failure. A gate resistance of 5.6 Ω was selected for the device under test (DUT). Resting time between pulses was sufficiently large (≥ 3 min) allowing the junction temperature to stabilize to ambient condition. In Fig. 3, V_{DS} and I_D measurements are shown for varying capacitor charging voltages from 600 V to 900 V in 100 V increments except for device failure, shown in solid line, that occurred at a charging voltage of 975 V. Device failure, characterized by the loss of blocking voltage capability, was shown to happen just briefly after avalanche mode operation which lasted 1.12 µs.

Avalanche energy density, measured with respect to current density, J_{AV}, is shown in Fig. 4 on the left y-axis and bottom x-axis respectively; the right y-axis represents the avalanche energy, and the upper x-axis represents the corresponding avalanche current. The inlet plot has the same top and bottom x-axes, but shows the peak avalanche power density on the left y-axis and avalanche time duration on the right y-axis. The maximum tolerable avalanche energy density was calculated to be 8.8 J·cm^{-2} resulting from an avalanche energy of 2.84 J. Peak power density was 3.22 MW·cm^{-2} and the maximum avalanche time duration was 6.5 µs. During the avalanche regime, V_{DS} peaked at 15.8 kV and the maximum current density was shown to be 199.2 A·cm^{-2} at 63.8 A.

A more thorough understanding of the 10-kV SiC MOSFET robustness is established via comparison with 1.2-kV SiC MOSFETs; modern fabrication trends would suggest both devices are DMOSFET structure. Results of this comparison are shown in Fig. 5. Device A represents the device evaluated in this work and Device B and C represent devices evaluated in [33]. Each measurement was obtained at 22 °C using a 1.42-mH load inductance. Device A was measured up to 8.8 J·cm^{-2}, Device B up to 7.59 J·cm^{-2}, and Device C up to 7.22 J·cm^{-2}.