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Time-zero-variability and BTI impact on advanced FinFET device and circuit reliability

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ABSTRACT

In this study a careful analysis of the device and the circuit level variability and reliability are presented. Planar 20 nm System on Chip (SoC), 16 nm FinFET (16FF) and 10 nm FinFET (10FF) devices are studied to understand the time-zero process variability and Bias Temperature Instability (BTI) stress induced (time dependent) threshold voltage (V_T) variations to evaluate the device degradation. Moreover, to understand the circuit level variability, the 6-Transistor (6T) SRAM performance is assessed in terms of the static noise margin (SNM) degradation under the influence of BTI stress. Finally, the product level SRAM performance is studied in terms of the minimum SRAM operating voltage (Vmin) degradation.

1. Introduction

Aggressive scaling of the transistor dimension to keep up with Moore's law has been a great challenge in the past decade [1–6]. Higher circuit density with better performance is becoming more difficult to achieve with each scaled node and hence, device to circuit reliability has become the crucial aspect of overall technology qualification [7–8]. Transistor scaling was possible using planar architecture until 20 nm technology node [2], but the short channel effects [9] limits the scaling to lower nodes with similar approach. Further scaling to 16 nm was possible using the FinFET architecture [3–4] as compared to the planar transistor. 16 nm FinFET (16FF) showed incredibly better electrostatic control which enabled better low power and high performance applications [3–4,7–8]. However, the time-zero process variations were introduced in the complicated FinFET (FF) process technology; such as having ⟨100⟩, ⟨110⟩ orientations, Fin height and width control issues etc. and hence the overall device reliability evaluation became even more onerous. This also calls for careful inspection of the circuit reliability in 16FF (and below) while benchmarking the product level performance.

In this paper, a detailed study is presented by comparing various device and circuit reliability matrices between high-k metal gate (HKMG) planar technology (20 nm System-on Chip, 20SoC) [2] and standard HKMG 16FF technology [3]. Time-zero threshold voltage (V_{T0}) variation is measured and the bias temperature instability (BTI) impact on threshold voltage (V_T) is also studied for these two technologies. Negative BTI (NBTI) for P-MOSFETs and positive BTI (PBTI) for N-MOSFETs are evaluated and their statistical behavior is compared. For NBTI induced V_T variability analysis, the 10 nm FinFET (10FF) [10] is also used. The overall BTI impact on SRAM circuit is evaluated in terms of static noise margin (SNM) degradation. Finally, the chip and bit level High-Temperature Operating Life (HTOL) test results are discussed in terms of Vmin degradation for SRAM and logic products. This work gives an overall picture of device to circuit to product level reliability using the advanced planar and FinFET process technology.

2. Device V_T variability and BTI impact

Process related variability is a big concern in any scaled technology and hence time-zero behavior needs careful attention. Variation of pre-stress or time-zero threshold voltage (V_{T0}) is plotted for 20SoC and 16FF technologies for P-MOSFET and N-MOSFET in Fig. 1(a) and (b), respectively. It can be seen that the V_{T0} dispersion is lower for 16FF as compared to 20SoC devices. The standard deviation (σ: sigma) indicates that how widely the variable (V_{T0} here) is distributed and in this case the V_{T0} sigma for 16FF is less than the 20SoC devices. This is the case for both N and P-MOSFETs and lesser dispersion (i.e. lower σ) can be attributed to the better gate electrostatic control for FinFET devices as compared to the planar technology [3–4].

To understand the time dependent V_T variability, the BTI induced pre- and post-stress V_T distributions are shown for 16FF in Fig. 2(a) for NBTI and in Fig. 2(b) for PBTI stress. The stress conditions are kept consistent here for fair comparison. In both cases, the V_T increases with

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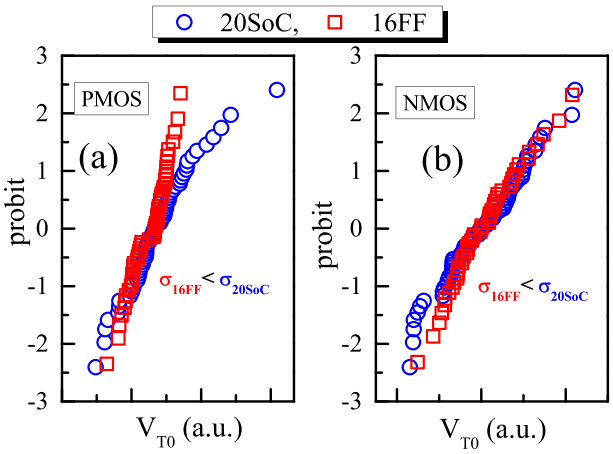

Fig. 1. Time zero threshold voltage (V_{T0}) variability is shown for (a) P- and (b) N-MOSFET devices for 20SoC and 16FF technology nodes.

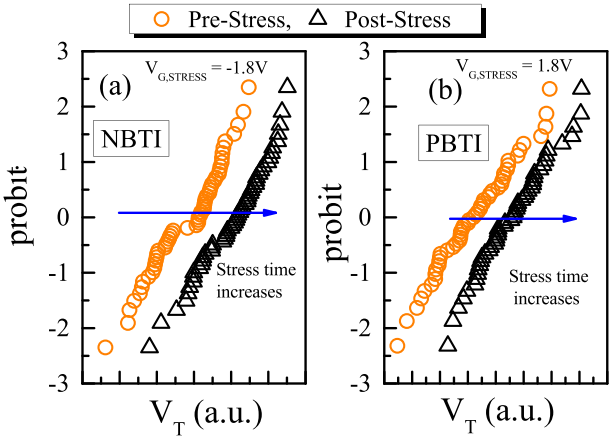

Fig. 2. Threshold voltage (V_T) distribution for pre-stress and post-stress conditions is shown for (a) NBTI and (b) PBTI stress for 16FF devices.

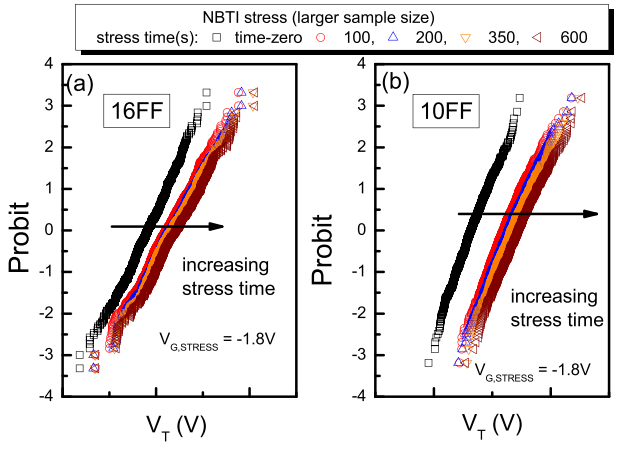

Fig. 3. V_T distribution is shown for NBTI stress for a larger sample size for (a) 16FF and (b) 10FF technology nodes. With stress, mean V_T changes, but sigma remains similar.

BTI stress, but the V_T distributions are almost parallel to each other; meaning that even if the absolute mean (μ) value of V_T changes, the dispersion (σ) of V_T does not change much with the stress time. This indicates that the V_T dispersion after stress is dominated by the sigma of initial V_{T0} distribution. To investigate more, a larger sample size V_T

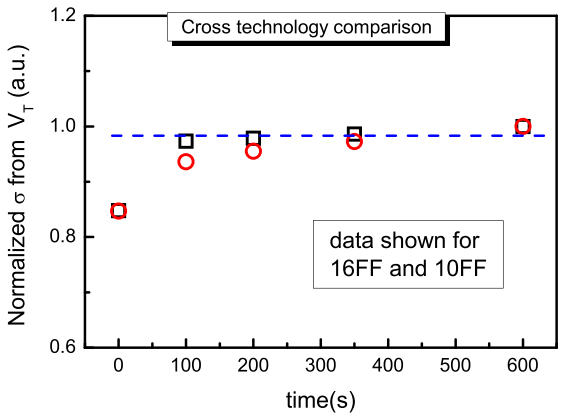

Fig. 4. Extracted σ from NBTI induced V_T is shown for 16FF and 10FF for various stress times. Both seemed to be invariant with time and indicate the influence of initial variability in overall degradation.

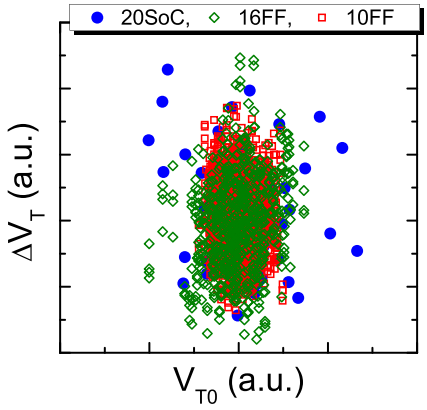

Fig. 5. Time zero threshold voltage is plotted against NBTI induced V_T shift for different technology nodes. Both parameters are normalized to mean values and the absolute V_T shift is seen to be uncorrelated to V_{T0}.

data (~1 k devices) for PMOSFET devices under NBTI stress is shown in Fig. 3(a) for 16FF and in Fig. 3(b) for 10FF technology nodes. In both cases, the V_T distribution is seen to be parallel, only having increasing mean V_T values with increasing stress conditions. The extracted sigma (σ) from V_T is plotted for different stress time in Fig. 4 and it is seen to be time independent for both FinFET technologies. Such exercise confirms the dominance of time zero variability in BTI induced overall V_T variability. This is also observed in some other reports [10–11]. Note that, ideally the variation of V_T should depend on the variance of V_{T0}, mean and sigma of ΔV_T and possibly on the correlation between V_{T0} and ΔV_T. But in this particular case, the sigma of V_{T0} is larger than the sigma of ΔV_T, which means that the variation of resultant V_T ($V_T = V_{T0} + \Delta V_T$) would be controlled by the V_{T0} sigma. Also it needs to be kept in mind that, the data is dominated by the intrinsic BTI degradation and does not suffer any tailing issue in the distribution which can be expected in product level variability due to other extrinsic factors. Such aspect of device to product level variability needs careful attention and will be discussed elsewhere. Investigating this further, Fig. 5 plots the NBTI induced ΔV_T shift against the initial V_{T0} values for 20SoC, 16FF, 10FF devices. Here both V_T shift (ΔV_T) and V_{T0} values are normalized to the respective mean values and no correlation is observed, i.e. the absolute V_T shift is independent of V_{T0}. It is similar to other reports [12–13]. The largest V_T shift occurs near the median V_{T0} value and the variation of FinFET device is seen to be least, which again supports the better process control for the FinFET devices as compared to planar devices.