Fast identification of true critical paths in sequential circuits

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ABSTRACT

The recent advancements in the implementation technologies have brought to the front a wide spectrum of new defect types and reliability phenomena. The conventional design techniques do not cope with the integration capacity and stringent requirements of today's nanometer technology nodes. Timing-critical paths analysis is one of such tasks. It has applications in gate-level reliability analysis, e.g., Bias Temperature Instability (BTI) induced aging, but also several others. In this paper, we propose a fast simulation based technique for explicit identification of true timing-critical paths in both combinational and sequential circuits to enable reliability mitigation approaches, like selecting the paths for delay monitor insertion, resizing delay critical gates or applying rejuvenation stimuli. The high scalability of the method is achieved by using a novel fast method for finding activated paths for many test patterns in parallel, a novel algorithm to determine only a small subset of critical paths, and a novel method for identifying the true critical paths among this subset, using branch and bound strategy. The paper demonstrates efficient application of the proposed technique to gate-level NBTI-critical paths identification. The experimental results prove feasibility and scalability of the technique.

1. Introduction

The conventional design techniques do not cope with the integration capacity and stringent requirements of today's nanometer technology nodes. Timing-critical paths analysis is one of such tasks. It has applications in gate-level reliability analysis, e.g., Negative Bias Temperature Instability (NBTI) induced aging being the dominant effect below the 65 nm technology node [1,2]. Explicit identification of true critical paths enables reliability mitigation like delay monitor insertion, resizing of delay-critical gates, or proper application of rejuvenation stimuli.

A wide range of academic [3–13] and commercial (including from EDA vendors like Synopsys and Cadence) solutions for critical path identification targeting combinational portions of circuits have been proposed over the previous decades. The simplest solution for finding the longest paths in the circuit is static (or topological) timing analysis (STA) which is highly scalable having linear complexity [3]. However, STA does not take into account sensitization aspects and thus provides generally overly pessimistic estimates for the length of paths within the core [4,5]. Functional Timing Analysis (FTA) overcomes the above shortcoming by utilizing automatic test pattern generation (ATPG) [6,7] or Boolean satisfiability (SAT) [7] based methods for generating true (functional) paths. On the other hand, the FTA methods are based on counting of all the paths in the circuit, and hence, unfortunately, are not scalable for using in real complex combinational circuits, not to speak at all of sequential circuits.

The problem of true paths identification has been addressed in the design field for delay computing and estimating the critical delays [3–7], and in the test field for generating tests with high path delay fault (PDF) coverage [8–13]. In design timing analysis [4–7], the main target is to compute the maximum possible delay in the circuit, where the explicit identification of the longest true paths is not needed. Such an approach avoids the labor intensive counting of paths in the circuit. To cope with the complexity of calculations, in [5], hierarchical approach is proposed where, however, only combinational circuits were discussed.

In [8–10], the critical path analysis problem is handled as the PDF testing task. In [8], individual PDFs are represented as combinations, and tested PDFs are represented as a combinational set in an implicit manner without enumeration of paths in the circuit. The approach is based on using zero-suppressed BDDs (ZBDD). In [10] a novel approach for timing analysis is proposed, based on the concept of identification of primitive PDFs. The method has the target to select a subset of path sets that determine the circuit output stabilization time. For efficient calculation of the number of critical primitive PDFs, ZBDDs are used, which allow implicit and compact representation of paths in the circuit. All these PDF-testing related methods are calculating only the PDF coverage, and are not targeting the search of explicit critical paths.

Statistical methods for the longest path selection in PDF testing are considered in [11,12]. In [11], a method to generate the longest path set for delay testing under process variation is proposed where a novel

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path-pruning technique is used to discard paths that are not the longest. In [12], a new path selection problem as an optimization problem is formulated. The method has the target to maximize the topological coverage of selected paths using the idea of path correlation. As in other PDF testing methods, the main targets of these methods are either path coverage calculation, or computing of the path delay distribution. No explicit identification of the longest paths is addressed.

Differently from the previous references, where mainly the delay of the critical path has been the objective, and not the critical path itself, the paper [13] has the target of explicit critical path extraction. In the paper, a method is proposed for identification of the longest path, and for generation an input pattern that sensitizes this path. However, only small combinational circuits (ISCAS'85) were experimented, the scalability of the method was not discussed.

2. Problem discussion

In the papers referenced above, only combinational and no sequential circuits were considered. However, in true critical path selection in combinational parts of globally sequential circuits, it is important to consider the critical paths in the context of sequential functionality, as there may be paths in the combinational parts that become false due to invalid state transitions (considered as *sequentiality constraints*). Therefore, scalable methods for true critical path identification in the general case of sequential circuits are needed, in particular, in the context of identifying aging critical paths in larger circuits. Note, differently from the case of combinational circuits, application of FTA based on the ATPG is not feasible for sequential circuits due to the extremely poor scalability of sequential ATPG.

In this paper, we consider the problem of identifying the longest critical paths in sequential circuits, seen as a "sea of gates", i.e. in cases where the high-level functional partition of the circuit is not available and the state transition diagrams are not given. In case of combinational circuits, the critical paths are identified by sensitizing them one by one in descending order of their topological (static) length if they can be sensitized. In sequential circuits, we have to deal with sequential paths where a path is a concatenation of several combinational paths (segments) in the iterative array model of the sequential circuit. The first segment of a sequential path begins at a primary input and the last segment terminates at a primary output. Hence, the number of paths in sequential circuits will grow up exponentially. In general case, this number may become even unknown if the sequential depth is high. In these cases, the traditional approach of using SAT for identifying the longest true critical paths will be unrealistic.

The Fig. 1 illustrates the difficulty of deterministic sensitizing of paths in sequential circuits. The presented circuit consists of three combinational sub-circuits CC_k and a sequential part SC. To sensitize

Fig. 1. Hard-to-sensitize path in a sequential circuit. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

the selected blue path through the combinational circuits CC1 and CC2, a dedicated (red) path has to be sensitized, which depends on a state of the block SC, which may need for initialization a very long hard-to-generate input sequence.

The task of sensitizing critical paths in sequential circuits may be manageable if the sequential depth of the circuit is not very high. However, at a certain limit of this depth, SAT-based deterministic methods of path sensitizing in sequential circuits are not feasible any more. The motivation of the present work is to fill this gap.

In the cases, when the SAT based deterministic approach is infeasible, and when the structural high-level information for guiding the sensitizing process is not available, the only way to identify the longest true paths is simulation-based search approach. It consists of the analysis of as many randomly generated sequential paths as possible. To guarantee the needed quality of the search, so that the set of identified critical paths can be qualified as a representative set, we have introduced statistical measures for evaluating the sizes of asymptotic errors in determination of longest true critical paths.

On the other hand, there are often many long true critical paths in circuits with rather similar length. In these cases, the probability of finding at least one of them will be the higher the bigger is the set of the longest true critical paths. This probability will grow when the number of simulated paths will grow.

The simulation-based approach is well suitable for identification of critical paths in mission critical circuits dedicated for running special routines as workloads. In these cases, the sequences produced by the mission critical workloads can be used for determining the sets of representative true critical paths.

To avoid the timing analysis of full sequential paths, we propose a method of analysis of only the combinational paths as segments of related certain sets of full sequential paths, without paying direct attention on the real possible sequential paths, which may include the segment. These sets of sequential paths are taken into account indirectly during logic simulation. For that purpose, first, we identify all the feasible states of the sequential circuit for the random input sequence by logic simulation, and then carry out the timing analysis of the feasible combinational paths in the iterative array model of the sequential circuit using the states as constraints for the analysis.

To formulate the problem, consider Fig. 2 which distinguishes between three subsets of all static paths in a given sequential circuit, where *NF* contains all static structural paths not functionally sensitizable due to sequential constraints, *NS* contains the rest of all not sensitizable static structural paths, and the set of all true paths, among which the longest ones should be selected. The dots P_1, P_2 and P_3 represent here the longest paths in these subsets with corresponding lengths: *Length* $(P_3) < $ *Length* $(P_2) < $ *Length* (P_1).

To make the search for the longest true path more efficient, first of all, the subset *NF* can be excluded from the search procedure by simulation of the whole sequential circuit, and thereafter the search can be started only in the remaining subset of paths.

Fig. 3a illustrates an example of a sequential circuit with two D-flip-flops, and with highlighted static structural paths P_1, P_2, and P_3.

Consider first, the path P_1 (shown by red bold lines) in the combinational part of the circuit, which starts at the output of the flip-flop T_1 and ends with the primary output y. P_1 is the longest static structural path in the circuit, however, the transition $1 \rightarrow 0$ cannot be sensitized on this path due to the redundancy in logic. Hence, P_1 is a false path.

Consider now in Fig. 3a the path P_2 from the output of flip-flop T_1 back to its input, which is highlighted by bold dash lines. The transition $1 \rightarrow 0$ on this path can never happen in this sequential circuit, because the needed initial state for this transition $\{T_1 = 1, T_2 = 1\}$, is illegal. Hence, this path belongs to the subset *NF*, and should be classified as false due to the sequential constraints.

In Fig. 3b, the relationship between the paths P_1, P_2 and P_3 in the combinational part of the sequential circuit is illustrated. If we would search for the longest path in this c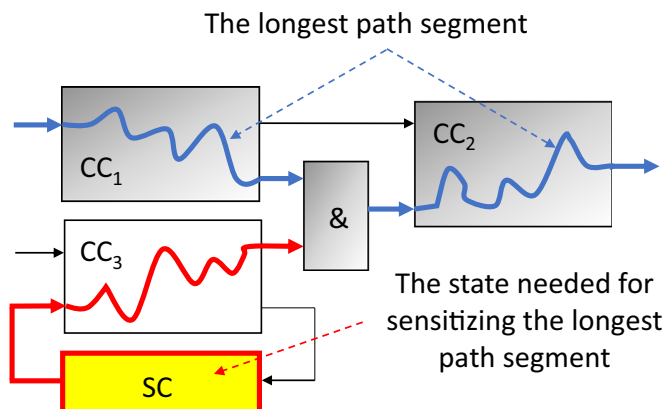ircuit, assuming the inputs $Q' = \{T_1,$