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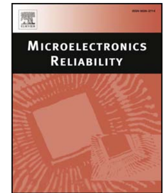
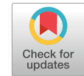


Invited paper

Integrated modeling of Self-heating of confined geometry (FinFET, NWFET, and NSHFET) transistors and its implications for the reliability of sub-20 nm modern integrated circuits



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ABSTRACT

The evolution of transistor topology from planar to *confined geometry* transistors (i.e., FinFET, Nanowire FET, Nanosheet FET) has met the desired performance specification of sub-20 nm integrated circuits (ICs), but only at the expense of increased power density and thermal resistance. Thus, self-heating effect (SHE) has become a critical issue for performance/reliability of ICs. Indeed, temperature is one of the most important factors determining ICs reliability, such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), and Electromigration (EM). Therefore, an accurate SHE model is essential for predictive, reliability-aware ICs design. Although SHE is collectively determined by the thermal resistances/capacitances associated with various layers of an IC, most researchers focus on isolated components within the hierarchy (i.e., a single transistor, few specific circuit configurations, or specialized package type). This fragmented approach makes it difficult to verify the implications of SHE on performance and reliability of ICs based on confined geometry transistors. In this paper, we **combine** theoretical modeling and systematic transistor characterization to extract thermal parameters at the transistor level to demonstrate the importance of multi-time constant thermal circuits to predict the spatio-temporal SHE in modern sub-20 nm transistors. Based on the refined Berkeley Short-channel IGFET Model Common Multi-Gate (BSIM-CMG) model, we **examine** SHE in typical digital circuits (e.g., ring oscillator) and analog circuits (e.g., two-stage operational amplifier) by Verilog-A based HSPICE simulation. Similarly, we **develop** a physics-based thermal compact model for packaged ICs using an effective media approximation for the Back End Of Line (BEOL) interconnects and ICs packaging. We integrate these components to **investigate** SHE behavior implication on ICs reliability and explain why one must adopt various (biomimetic) strategies to improve the lifetime of self-heated ICs.

1. Introduction

Transistors and ICs have been scaled down continuously under Moore's law to achieve better performance at a lower cost [1,2]. Scaling of transistors decreases both power dissipation and the intrinsic switching time so that a densely-packed, high-speed circuit can operate with modest self-heating. However, short channel effect (SCE) arising from ineffective gate control makes sustained scaling difficult [3,4]. The deterioration of the subthreshold swing (SS) increases off-state leakage current (e.g., threshold voltage (V_{TH}) roll off), with the corresponding increase in the static power dissipation. In order to reduce the SCE, transistor topology has been modified to obtain a good electrostatic control of its channel. Multi-gate (MG) transistors, such as FinFET, gate-all-round (GAA) nanowire (NW) FET, [5–8], and Floating body structures, such as extremely-thin-silicon-on-insulator (SOI)-FinFET [9–11] have been introduced and the structures have successfully minimized the SCE.

The introduction of confined geometry, multi-gate transistors has allowed scaling to continue below the 20 nm-node. Unfortunately, leakage current and V_{TH} have not been scaled, therefore there has been a net increase in power density as ICs have become smaller. Thus, the rise in the transistor channel temperature (ΔT), defined by the product of the power dissipated within the channel (P) and the thermal resistance of the material system surrounding the channel (R_{TH}), has become one of the most important performance limiters of modern ICs, restricting practical processor frequency (f) to around 4GHz [12].

Self-heating effect (SHE) has a detrimental effect not only on the performance but also on the reliability, such as Negative Bias Temperature Instability (NBTI), and Hot Carrier Injection (HCI) of a transistor, electromigration (EM) of the interconnect lines, etc. If the

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temperature dependence of a degradation process is given by an Arrhenius relationship:

$$R = R_0 e^{\frac{-\Delta H}{kT}}. \quad (1)$$

(Here R_0, ΔH, k, and T are the extrapolated degradation rate at absolute zero temperature, the activation energy of the corresponding process, Boltzmann constant, and the absolute temperature, respectively), only a 30 °C rise in temperature (for a process with $\Delta H = 1eV$) will increase the degradation rate hundred-fold! Indeed, bond dissociation rates for NBTI and HCI, or diffusivity of Cu atoms that dictates electromigration (EM) cannot be modeled unless transistor SHE is quantified.

As the channel length becomes smaller (e.g., sub-20 nm), and the channel topology more confined, SHE increases due to the following reasons. Confined geometry transistors ensure excellent electrostatics, only at the expense of increased R_{TH} very close to the heat source. Furthermore, new high-mobility channels (i.e., SiGe, Ge) [13–16] and high-K gate dielectrics (i.e., HfO_2) [17,18] have been developed to increase on-current at lower voltage and to reduce gate leakage, respectively. Unfortunately, high mobility and high-K materials have lower thermal conductivities (κ), which further increase channel $R_{TH}(\sim \kappa^{-1})$. In other words, confined geometry transistors shift the burden of transistor design from electrostatic control to the management/control of thermal effects.

Another crucial issue for scaled transistors is the decreasing time constant (τ_C) for self-heating. As the channel volume is reduced, thermal capacitance (e.g., $C_{TH} \equiv \rho \cdot c_P \cdot V$, where ρ, c_P, and V are the density of the material, specific heat, and volume, respectively) becomes extremely small as well. Consequently, the channel heats up much faster (with reduced time constant, $\tau_C \equiv R_{TH} \cdot C_{TH}$) than it used to for long channel planar transistors. When the slew rate is low, the effect of the small τ_C may be neglected, however, when the slew rate is high, the channel will heat up quickly to its steady-state temperature at sub-ns timescale. This thermal time-constant issue (a circuit may actually be described by several time-constants [19]) must be accounted for sub-20 nm high-speed ICs. Indeed, the importance of thermal-aware transistor and circuit designs has been highlighted by many groups to address issues regarding performances, variability, and reliability of confined geometry transistors.

In order to predict the reliability of a fully packaged IC, one must simultaneously consider hierarchical heat dissipation through the transistor channel and contacts, Back End Of Line (BEOL) interconnects, and the package. Many groups have developed tier-specific thermal models, which can neither predict the channel temperature rise (ΔT_C) accurately nor suggest innovative strategies to reduce ΔT_C by identifying/removing thermal bottlenecks in the hierarchy. Experimental observations from an isolated level may actually mislead and not correlate at all to the actual performance and lifetime of the ICs. For example, the floating-body transistor under DC operation may show severe self-heating. However, the self-heating extracted from the circuit simulation shows that the temperature rise is negligibly small (below 5 °C), as reported in [20,21]. When considering the effect of BEOL, the coupled SHE behavior may get worse or better depending on the relative importance of additional heat dissipation pathways vs. additional Joule heating in BEOL [22]. In short, fragmented focus on isolated components leads to confusing conclusions.

This paper develops a new methodology to calculate R_{TH} and C_{TH} in each level of the hierarchy and then combine them through a thermal network to determine SHE behavior of the integrated system. The holistic model can estimate ΔT_C accurately, so that one can make reliable estimates for BTI, HCI, and EM lifetimes. The modeling framework developed in our previous work allows us to compare performance/reliability implications of different ICs structure, such as circuit type and its operating mode (i.e., digital or analog), interconnect and via configurations, and transistor topology (i.e., FinFET, NWFET, nanosheet FET) [23]. Finally, we propose tier-specific strategies to reduce SHE and increase the lifetime of self-heated ICs.

This paper is arranged as follows: In section II, we introduce self-heating characterization methods for the transistor, verify the heat dissipation pathways, and then extract thermal parameters by numerical simulation. In section III, we investigate the self-heating in the digital and analog circuits. In section IV, we demonstrate the methodology to calculate precise temperature within BEOL and Front End Of Line (FEOL) for a packaged IC based on newly developed thermal compact modeling (TCM) technique and show how to couple TCM for each tier to obtain the reasonable estimate for ΔT_C. In section V, we discuss how NBTI, HCI, and EM affected by SHE and in section VI, we suggest several innovative solutions for each tier to increase the lifetime of ICs.

2. Device characterization

2.1. Experimental methodologies

In order to analyze the SHE from the transistor to the system level, we must first begin with the characterization of the channel temperature. The electrical characterization methods include AC output conductance and pulsed I—V methods. Basically, the channel temperature is obtained by comparing measured currents under AC and DC biases, and translating this difference to channel temperature through a (chuck-temperature vs. DC current) calibration curve [24]. We have used these techniques to analyze self-heating in transistors with different topologies, such as the number of Fin or NW, channel width, and channel length. For example, as the number of Fins or NW increases, SHE increases due to thermal cross-talk between the fins, as shown in Fig. 1a.

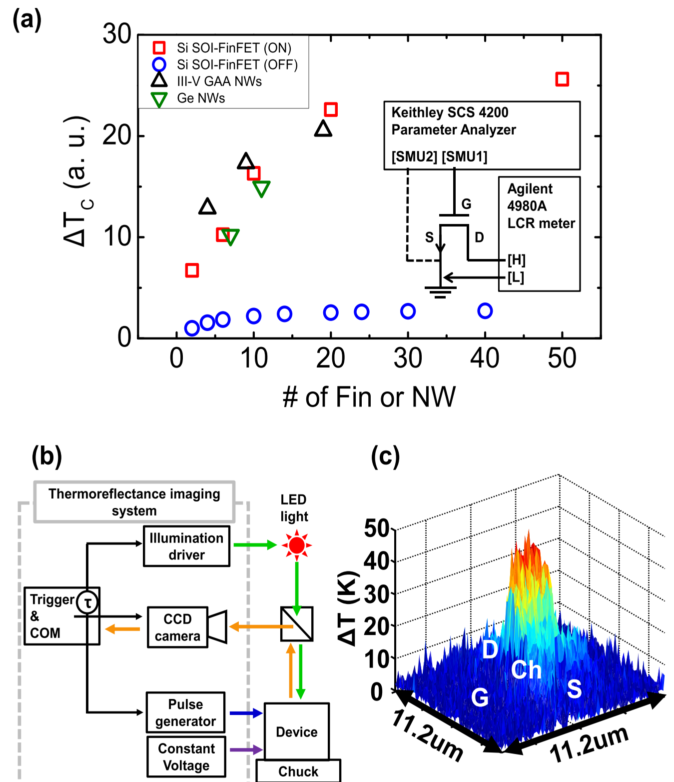

Fig. 1. (a) ΔT_C depends on the number of Fins and NWs for floating body structures such as SOI-Fin [25,26], GAA NW, and Ge NW [27]. The range of ΔT_C depends on the specific transistor technology, therefore [a.u.] is used to highlight the fact that SHE increases with fin-number and related thermal cross-talk. (inset) AC output conductance setup. **(b)** Optical self-heating characterization setup (thermos-reflectance). **(c)** A surface thermal image of a transistor.

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