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Modeling the impact of well contacts on SEE response with bias-dependent Single-Event compact model

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ABSTRACT

With technology scaling, a common and efficient strategy to improve the soft error vulnerability of sensitive nodes is to place well/substrate contacts frequently. This paper reports a revised method to integrate the impact of well contacts on SEE response with the bias-dependent SE compact model for circuit simulation. After modifying the SE sub-circuit with resistors and current source placed between the n-well and p-well contacts and then calibrating the parameters by layout-level TCAD simulation results, the resulting model is able to evaluate the SEE vulnerability of devices and circuits with various well contacts. Besides, it is able to evaluate the hardness performance of well contact optimization before fabrication.

1. Introduction

To evaluate the Single Event Effects (SEE) vulnerability of sub-100 nm circuits, the choice of strike kernel model plays a critical role [1]. Various bias-dependent Single Event (SE) models, usually developed through calibration based on TCAD mixed-mode simulation results, have attracted much attention [2–4]. In sub-100 nm CMOS technologies, charge sharing and well potential modulation have significant impacts on the single event response of devices and circuits [5–7]. For charge sharing effects, some researches deployed charge sharing models to describe the interaction between adjacent devices during one ion strike, by means of distribution table model or empirical functions derived from TCAD calibration data [1,8]. With technology scaling, a common and efficient strategy to improve the soft error vulnerability of the sensitive nodes is to place well/substrate contacts frequently [6,7]. The impact of well contacts has not yet been introduced in bias-dependent SE models, since the TCAD calibration is usually done for specific well contacts [2–4]. As a result, it is difficult to evaluate the precise response to various contact configurations in real layout design and its impact on radiation hardness.

This study is focused on integrating the impact of well contacts with bias-dependent SE compact model for circuit-level prediction. We aim to discuss the contribution of well contacts in predicting the transient shape of SE pulse and present the procedure to quantitatively extract parameters used in the resulting sub-circuit. The results agree well with the layout-level TCAD simulation results of inverters. In this way, we may evaluate the SEE vulnerability of devices and circuits with various well contacts, to check the hardness performance of well contact optimization before fabrication.

2. Influence of well contacts

Referring to [1–4] [8], the first step to build a bias-dependent SE model is to get the mixed-mode simulation results with nMOSFET represented by TCAD structure and pMOSFET represented by compact model. Thus, it is reasonable to focus on the influence of p-well contacts to a greater extent.

Fig. 1(a) shows the TCAD structures of a Wp/Lp = 240/40 and Wn/Ln = 120/40 nm inverter for mixed-mode and layout-level simulations. The 3-D TCAD structures and doping distributions were calibrated with a commercial 40 nm CMOS technology, the supply voltage (Vdd) equals to 1.1 V [9]. The TCAD and SPICE simulation results in Fig. 1(b) suggest that the mixed-mode and layout-level simulations can both produce good estimation of the electrical characteristics.

However, when simulating the SEE response of the inverter with an LET = 30 MeV·cm^2/mg heavy ion striking at the nMOS drain region, mixed-mode and layout-level simulations produce different voltage pulses (see Fig. 2), mainly in the plateau voltage and the pulse duration.

Since both the simulations have included the impacts of well potential modulation and the resulting bipolar amplification effect (with the same p-well contact), the cause of the differences should be related with the charge collection in the n-well region. In addition, considering

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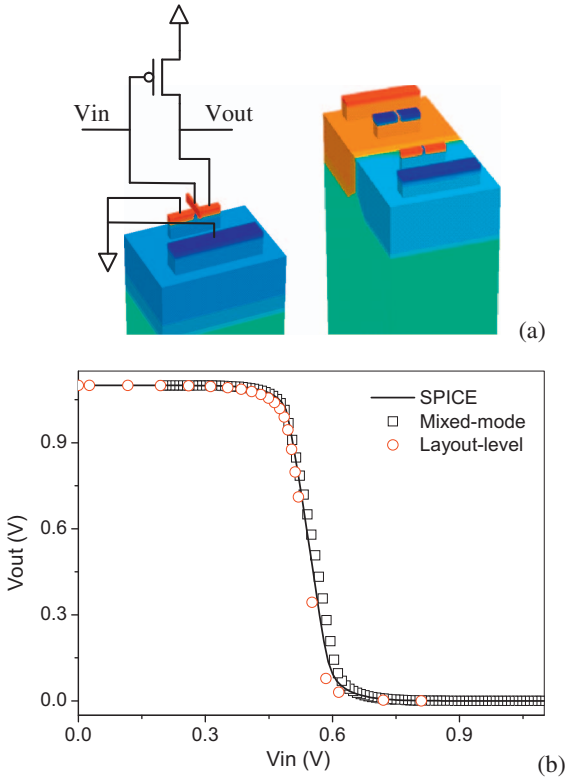

Fig. 1. TCAD structures for mixed-mode and layout-level simulations of a Wp/Lp = 240/40 nm, Wn/Ln = 120/40 nm inverter (a); TCAD and SPICE simulated transfer characteristics (b).

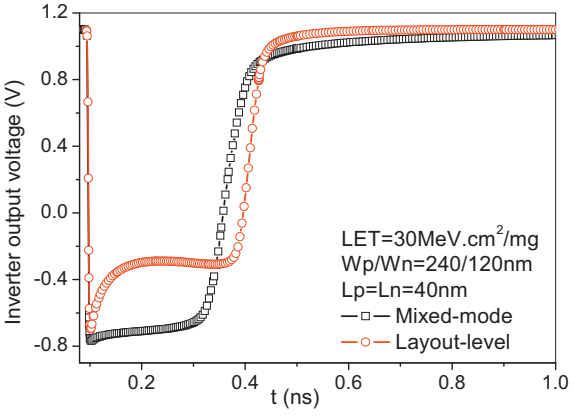

Fig. 2. Comparison of TCAD simulated SEE response of the Wp/Lp = 240/40 nm and Wn/Ln = 120/40 nm inverter produced by mixed-mode and layout-level simulations.

that both the drain and the source contacts of the pMOSFET are connected with high voltage, the charge collection in the n-well/p-well junction becomes the most possible reason. To confirm this, another TCAD structure for revised mixed-mode simulation was built as illustrated in Fig. 3(a). The 3-D TCAD model contained not only the p-well region and the nMOSFET but also the n-well region. The remaining pMOSFET was still represented by the compact model. Electrons distribution after the ion strike is also included in Fig. 3(a), it can be seen that the charge collection between n-well and p-well contacts did happen. From the results in Fig. 3(b), the revised mixed-mode simulation is able to produce very close results to the layout-level simulation, both in the plateau voltage and the pulse duration.

Therefore, it is necessary to include the impact of charge collection process in the n-well/p-well junction when building and utilizing the SE compact model.

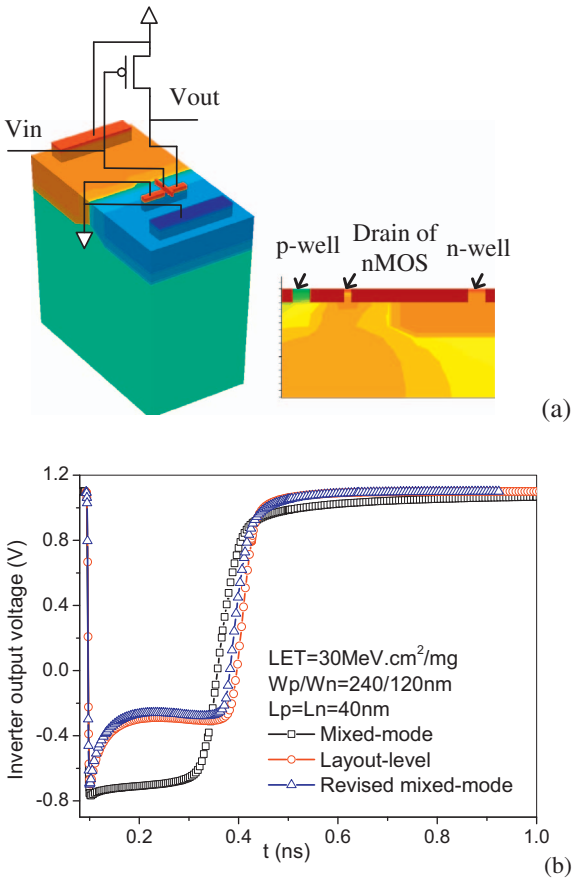

Fig. 3. Comparison of TCAD simulated SEE response of the Wp/Lp = 240/40 nm and Wn/Ln = 120/40 nm inverter produced by mixed-mode, revised mixed-mode and layout-level simulations.

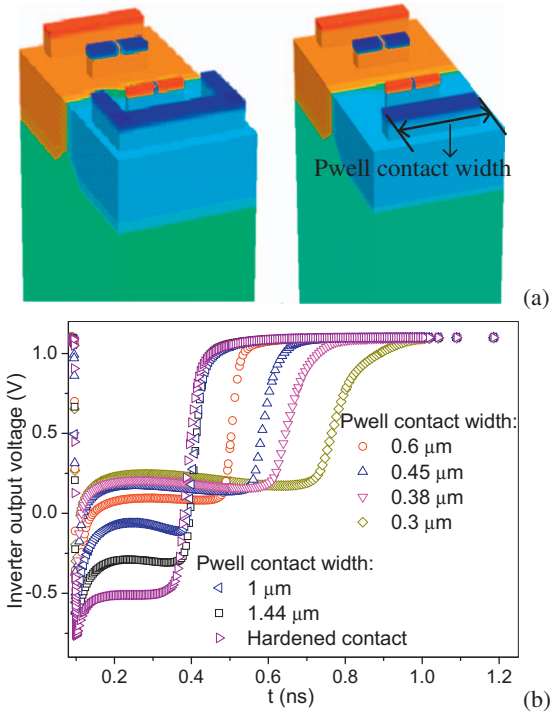

Fig. 4. 3-D TCAD structures of inverter with hardened p-well contact and strip contact of various contact widths (a); TCAD simulated output voltage pulses for LET = 30 MeV·cm²/mg strike at the nMOS drain region (b).