Microelectronics Reliability xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Investigations and detections on a new BEOL dielectric failure mechanism at advanced technologies

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ARTICLE INFO

Keywords:
BEOL
Low k dielectric
ILD
Failure mechanism
Test structure

ABSTRACT

The ultra-low k dielectrics have been widely used as semiconductor technology steps into 45 nm, 28 nm, and more advanced nodes. Combined with the rapid shrinks of critical dimensions, the ultra-low k dielectrics face challenges to retain the benefits of interconnect scaling both on their manufacturability and reliability performances. In this paper, abnormal failure phenomena were investigated on 28 nm ILD (Intra Level Dielectric) and IMD (Inter Metal Dielectric) qualifications and 40 nm mass production. A new failure mechanism of metal 1 to poly (M1-to-poly) leaky path was proposed based on theoretical investigations and experiments. Based on our newly proposed dielectric breakdown mechanism, a series of innovative test structures were designed for early detections and evaluations of reliability performances. These newly designed test structures have been proven to be useful due to better representing actual using profiles, more precise reliability evaluations, and more effective monitors on process variations at mass production.

1. Introduction

Device failure rate increases as technology marches to the 28 nm and more advanced nodes. The integration of advanced CMOS needs to be strengthened to meet continuous technical challenges on shrinking the critical dimensions [1–2]. As an important factor in the entire semiconductor manufacturing process, BEOL (Back-End of Line) dielectric reliability is essential for process reliability assessments. When the technology node steps down to 45 nm, 28 nm, and lower, it is inevitable that the manufacturers use ultra-low k (ULK) dielectrics. However, the introduction of ULK dielectrics in copper interconnects on the advanced nodes faces the challenges to retain both the benefits of their process windows and reliability performances [3]. The appropriate ULK materials, which offer an efficient solution to reduce signal delays, have to meet the requirements on thermo-mechanical properties, reliability performance, and BEOL processes. The reliability of ULK dielectrics has caught concerns in applications such as high speed circuits and capacitors, where high densities of interconnects are often mingled with biases. The ULK materials used in semiconductor devices must meet required operation lifetimes and should not suffer premature dielectric breakdowns [4,5]. In order to better understand the reliability performance of these ULK dielectrics, proper test structures need to be designed to accurately assess their reliability. The test structures should be designed to reflect actual chip layout and environments; the test structures should be also designed to facilitate the studies on intrinsic reliability [6].

In this paper, we investigated the abnormal failure phenomena of 28/40 nm ILD (Intra Level Dielectric) and IMD (Inter Metal Dielectric) dielectric breakdowns. A failure mechanism through metal 1 to poly (M1-to-poly) was proposed with theoretical explanations on the abnormal IV curves. The optimized ILD/IMD test structures were designed to exclude M1 to poly leaky path and to evaluate dielectric properties. A series of innovative test structures were designed and tested to detect and assess reliability based on the new BEOL M1 to poly dielectric breakdown mechanism. Using the innovative test structures, we are able to conduct adequate reliability qualifications on ULK dielectrics and precisely monitor process variations at mass productions.

2. Experiments

In this paper, all devices used for the ULK dielectric tests were fabricated using 40 nm or 28 nm Cu Dual Damascene processes. The ILDs were carbon-doped oxides (SiCOH k ≈ 2.75 & 2.55). The copper lines were surrounded by Ta/TaN barriers on the sidewall and at the bottom, capped by SiCN dielectric layers. A traditional metal comb-to-comb design, as in Fig. 1, was used to evaluate the ULK dielectrics. A voltage ramp (Vramp) test was applied on the ILD/IMD test structures at the temperature of 125 °C by a floating substrate.

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http://dx.doi.org/10.1016/j.microrel.2017.10.033
Received 2 June 2017; Received in revised form 25 October 2017; Accepted 28 October 2017

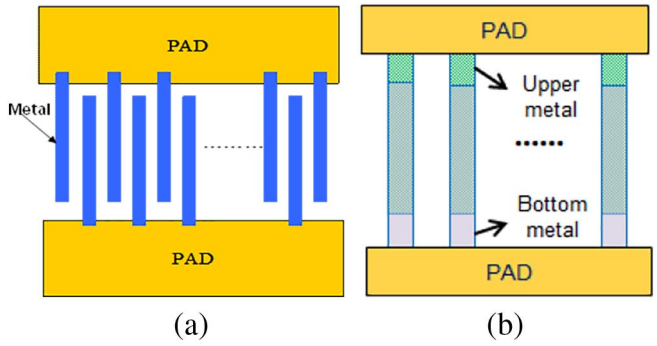


Fig. 1. Schematics of ILD/IMD structures: (a) intra level; (b) inter level.

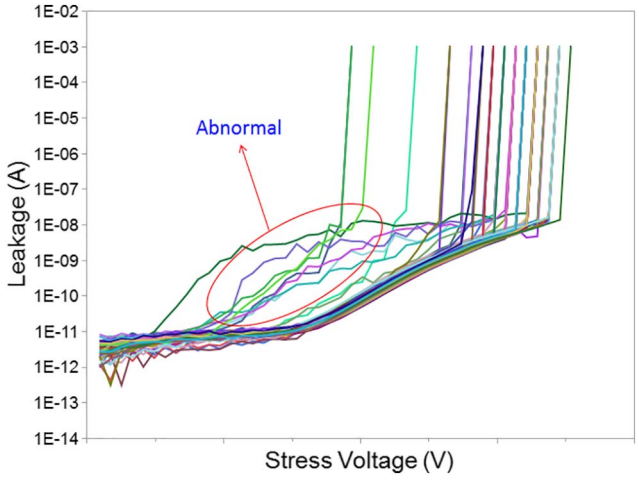
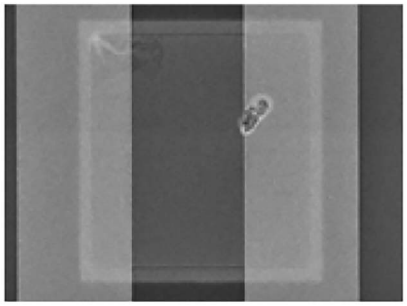


Fig. 2. The IV curves of a 28 nm ILD/IMD test.

3. Investigations on the failure mechanism

Due to the line-to-line degradation of the ULK dielectrics, ILD reliability is a major concern. Following the minimized design rules, as shown in Fig. 1, we use comb-to-comb and comb-to-serpentine structures for intra and Inter Metal Dielectric tests. Using these structures, we observed abnormal results as in Fig. 2. After conducting failure analyses (FA), we found the breakdown is not originated from the ILD/IMD, but underneath the test pads. Fig. 3 is the FA photo on a post Vramp abnormal sample. The TEM cross section showing the location of actual breakdown was in Fig. 3(b). M1-to-poly breakdown was observed by TEM, which points out the M1-to-poly leaky path in the ILD/IMD test.

The thickness of IMD becomes thinner with the shrinking critical dimensions. The IMD underneath the metal pads also follows the same trend. In our studies, the dummy poly underneath the metal pads formed a leaky path through the pad-to-pad as in Fig. 4. A series of capacitors C1 (between M1 and poly) and C2 (between poly and the active area, AA), under the pads as in Fig. 4, has to withstand a continuous electric field under voltage stress. The remaining thickness of SiN and ILD between M1 and poly and the thickness of gate dielectric were smaller than the minimum metal spacing to initiate the M1-to-poly breakdown. In this case, when the two pads were in series, the total dielectric thickness was close to the minimum metal spacing of the ILD structure. Considering the accumulation effects of the non-uniformity of IMD thickness after CMP (Chemical Mechanical Polishing), the metal trench etch, the poly thickness and the dielectric thickness between M1 and poly, there would be certain weak points. The insulator thickness was 16 nm at the wafer center and 31 nm at the wafer edge as in Fig. 5. The total dielectric thickness along the pad-to-pad path was less than the minimum metal spacing in ILD structures. This



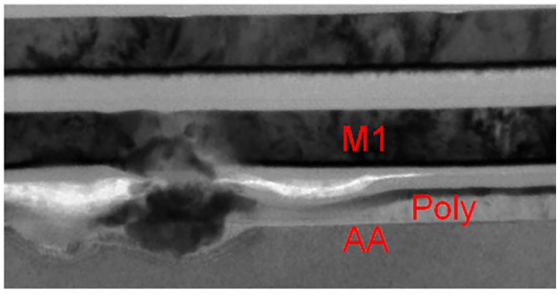


Fig. 3. SEM/TEM image of the breakdown underneath a PAD.

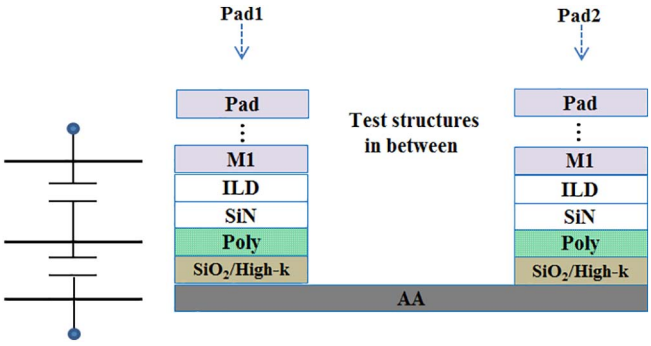


Fig. 4. A schematic of pad-to-pad leaky path and the cross-section: two capacitors in series under the pads.

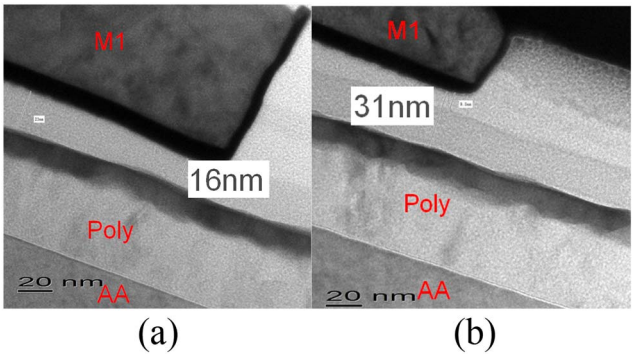


Fig. 5. The pad TEM cross section under M1: (a) wafer center; (b) wafer edge.

explained why breakdown was originated under the pads instead of the originally designated areas on ILD/IMD test structures.

To verify the proposed failure mechanism and the leaky path between the pads, we applied ramp voltages on two adjacent pads without test structures at 125 °C and room temperature. The IV curves are shown in Fig. 6. Based on the above discussion and the schematics in Fig. 4, we can easily explain Fig. 6, whose abnormal IV curves can be