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Study of proton radiation effect to row hammer fault in DDR4 SDRAMs

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ABSTRACT

This paper shares the effects of row hammer fault through high-energy proton radiation. The significance of row hammer fault is highlighted in terms of two different technologies in DDR4 SDRAM.

Row hammer stress prevents nearby storage cells from maintaining storage data within the retention time of 64-ms. The stress is worsened by the radiation damage in silicon due to the high-energy particles.

Proton-based radiation damage tests were performed with DDR4 SDRAM components from two different technologies. Experiment results showed that after proton irradiation, the number of bit errors caused by the row hammering test increased about 41% and 66% in technologies 2x-nm and 2y-nm, respectively. With 2y-nm technology, bit errors started to appear from 5 K Number of Hammering (N_{HMR})—the equivalent of 500-μs retention time. For 2y-nm components, more than 90% of failed words had multiple failed cells, which could not be corrected by Single Error Correction and Double Error Detection (SEC-DED) codes.

1. Introduction

Synchronous Dynamic Random Access Memory (SDRAM) allows for high densities of storage cells within limited areas, which helps attain: 1) high-speed operating frequencies through Double Data Rate (DDR), and 2) low power consumption through Low Power DDR (LPDDR). Recently, manufacturers introduced DDR4, which can operate at a clock frequency of 2133 MHz—52.3% faster than DDR3, which can only operate at a clock frequency of 1400 MHz [1,2]. Furthermore, Single Event Effect (SEE) by high-energy particles was not a problem for SDRAM, even when the technology scaled, because of SDRAM's relatively large storage capacitance compared to other memory devices [3].

Researchers discovered that when a single row address is repetitively accessed, storage cells—which are physically adjacent to the accessed row—can be disturbed within 64-ms retention time, t_{RET}. This disturbance is referred to as row hammer or Active Precharge (AP) hammering fault [4–8]. Previous research showed that row hammer fault could occur through WordLine to WordLine (WL-WL) coupling and the adjacent gate effect [5]. With the adjacent gate effect, row hammer fault occurs when the channel charge—after the aggressor word line (WL_{AGGR}) deactivation—diffuses and drifts to recombine with the storage charge in the victim storage capacitor on the victim cell, which shares the same bit line with aggressor cell [7,13].

As technology scales down, the physical distance between adjacent wordlines narrows, and row hammer fault becomes problematic. Previous research showed that in DDR3, with 3x-nm technology, 200 K number of hammering (N_{HMR}) on the WL_{AGGR} was the minimum amount of accesses that could sustain data in victim cells [7]. 200 K N_{HMR} is only 15.4% of the maximum number—1300 K N_{HMR}—of repetitively allowed accesses on a wordline within 64-ms t_{RET}.

Fig. 1(a) shows the simplified logical structure for conventional SDRAM cells. Since there is intrinsic leakage current from storage capacitors, regular refresh operations are required to sustain stored data; a 7.8-μs refresh time interval (t_{REFI}) is recommended by Joint Electron Device Engineering Council (JEDEC) standards [2]. The behavior for row hammer fault can be modeled by an added leakage path from a memory cell shown as resistance, R_1, Fig. 1(a).

Radiation of energetic particles can physically damage transistors. Micro-dose or Displacement Damage (DD) by such radiation can aggravate the leakage current, which can be modeled by an additional leakage path shown as R_2, Fig. 1(b). The additional leakage caused by radiation damage can cause stuck bits, which refers to the cells that cannot hold their data for 64-ms t_{RET} [9–12]. The leakage path, R_1, by row hammer fault is not related to SEE or radiation damage, but can make compounding effect together with leakage current from cells damaged by radiation. In general, the neutron manifests the similar behavior with the high-energy proton; the proton based acceleration tests were performed to determine the accumulated radiation damage

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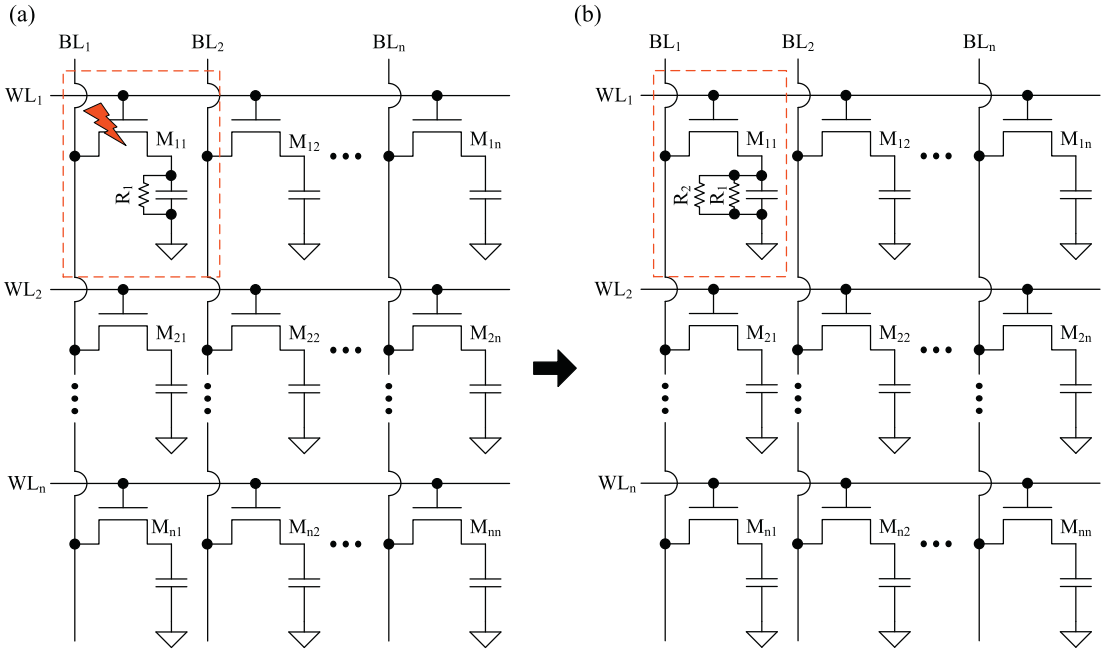

Fig. 1. Logical structure of conventional SDRAM and modeling of radiation induced damage; (a) is for pre-irradiation, and (b) is radiation damage at M_{11} after irradiation.

for expended period on the semiconductor devices [14]. The row hammering test was more useful than conventional retention tests in assessing reliability issues that comes with leakage from storage cells [13]. In this work, the weakness of DDR4 SDRAM is discussed in conjunction to row hammering stress. Also demonstrated, is how radiation damage aggravates row hammer fault in DDR4 SDRAMs.

The rest of this paper is organized as follow: Section 2 describes the experimental environment for the row hammering test and the proton irradiation test. Sections 3 and 4 compare the row hammering test results of DDR4 samples pre- and post-proton irradiation. Section 5 investigates row hammering test results between technologies. Section 6 concludes this work.

2. Experimental environment

2.1. Test platform

The Memory Tester was developed to conduct two types of tests: the proton beam radiation test and the row hammering test as shown in Fig. 2. The Memory Tester has three major parts: the main control board, the Device Under Test (DUT), and the host computer. The main control board implements hardware control logic using the Field Programmable Gate Array (FPGA). Two different Built-In Self-Test (BIST) engines were developed for two types of experiments: 1) JEDEC JESD89A-based BIST, which was used for the proton irradiation test, and 2) row hammer BIST, which was used for the row hammering test [7,15,16].

The Host Computer remotely controls test processes, and records test results by downloading buffered data in control hardware. The DUT components were connected to the main control board through an Unbuffered DIMM (UDIMM) interface, compliant with JEDEC standards [17].

Two types of DDR4 samples—2x-nm and 2y-nm—in two technologies from the same manufacturer were tested with high-energy proton; technology x is larger than technology y. The row hammer test was performed before and after radiation to see the effects of proton radiation damages. All DDR4 samples had 4-Gb capacity with 16 banks, 15 bits of row address, and 10 bits of column address with 3 bits burst address. All samples were tested with nominal voltage − 1.2 V for V_{DD} and V_{DDQ}. Manufacturer and part names are not disclosed due to a confidentiality agreement with Cisco Systems, Inc.

2.2. Proton beam radiation test

The UDIMM based DDR4 components were tested using a proton beam with 480 MeV energy at the TRIUMF facility shown in Fig. 3. Single rank DIMM card is custom-built for the radiation test to be compliant with JEDEC standard [17]. The card can accommodate the maximum of 8 × 8-DDR4 components. For a radiation and row hammering test, only two component are populated. Each component is

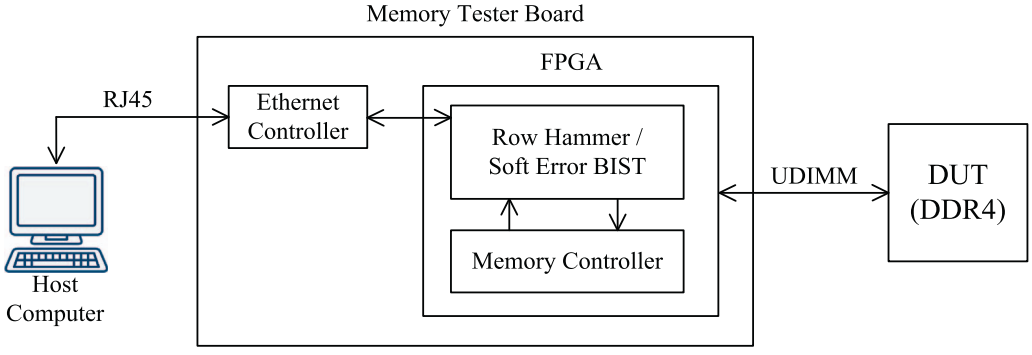

Fig. 2. Memory tester system with main control board, DUT, and host computer, to conduct two types of experiments: row hammer and proton irradiation experiments.