Ultra-low-voltage boosted driver for self-powered systems

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ABSTRACT

This paper deals with the ultra low-voltage design and application of an inverter-based driver. In order to ensure a reliable value of the overdrive voltage for transistors, the topology based on a boosting technique was used. The driver was designed in 130 nm CMOS technology and verified by simulations including technology corners and measurement of prototyped chips. The whole boosted driver achieves energy consumption of 92.12 μW for the load capacitor of 100 pF. Due to the low-power consumption and promising measured propagation delay, the designed driver was successfully implemented in a self-powered dynamic threshold charge pump. To ensure the reliable start-up, the minimum precharging voltage of the output capacitor has been investigated. The start–up conditions and achieved parameters were verified by measurement and compared to other related works. The optimum point for reliable start of the charge pump has been observed for the clock frequency of about 160 kHz, where the minimum start-up voltage of 126 mV is needed. In such a case, the start-up time is 1.05 ms and the output voltage of 379 mV will be reached.

1. Introduction

The essential requirements for an integrated circuit (IC) have always included performance, high reliability, small chip area and low costs. Nowadays devices like medical applications also require to be as portable as possible. Therefore, the total power consumption of such electronic systems needs to be kept low [1]. This can be effectively achieved if ICs are designed with a low value of the supply voltage. Such an approach brings in turn new trade-offs, while the low supply voltage highly constraints the circuit operation and performance. This effect becomes more significant in sub-micron technologies, where Process-Voltage-Temperature (PVT) variations increase. With a limited value of the supply voltage and reasonable size of design, the driving capabilities become very limited. This issue mainly includes two research areas:

- Interconnects parasitics in high–speed digital systems
- Driving high–load capacitances in analog systems

With rapid CMOS technology downscaling, on-chip global interconnects have become the bottleneck for high-speed operation due to the increase of the time constant RC per length of a wire. In turn, the time constant increases the global delay of wires. The low-voltage design techniques using the MOS transistors in sub-threshold region can reduce the total MOS gate capacitance (C_{GS}), since the channel depletion capacitance (C_D) appears in series with the oxide capacitance

(C_{OX}). Additionally, interconnect capacitance remains independent of the supply voltage value [2]. There are various process and circuit techniques to make the wire delay less proportional to the wire length [3–5]. However, according to the mentioned adversities, the global wire delay will further dominate over the logic (gate) delay, and it will represent the main performance limiting factor [2].

To cope with insufficiently high supply voltage, the switched regulators can be used to effectively compensate this limitation by converting a low value of the input voltage to an elevated voltage value at the output. One of the most popular solutions of switched regulators is a charge pump (CP) that is based on the switched-capacitor technique [1]. Since a CP usually utilizes rather large capacitors, it has to be ensured that the capacitors are reliably charged and discharged with digital clock signals. Accumulated charge is then sequentially propagated through switches to the output node that elevates its voltage higher.

2. Motivation

No matter what capacitance (load or interconnect one), its presence in the signal path requires special circuit design approach in order to preserve signal key parameters. Usually, an inverter-based driver can serve this demand. Fig. 1 shows the block diagram of a simple charge pump system employing inverter drivers (one for each clock signal - Clk_C and $nClk_C$). The driver then provides the corresponding driving clock signals at its outputs (Clk_D and $nClk_D$), which drive the signal over

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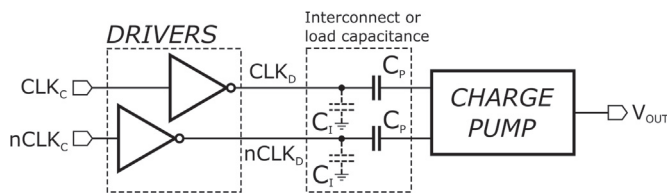
Fig. 1. The block diagram of a charge pump system.

Fig. 2. The concept of the boosted interconnect driver presented in [2].

either interconnect or CP capacitances. Design of such a driver has been solved as the essential part of our previous work [6]. The achieved parameters of the driver are also summarized in this paper, and one of the key parameters - the propagation delay has been also verified by measurement of the fabricated prototype chips.

Besides the driver performance in a wide range of load capacitances, we have also investigated its implementation as a part of an energy management unit for more complex systems such as self-powered or energy autonomous applications [7–9]. The photovoltaic cell [7], electromagnetic [8], piezoelectric [10] or electrostatic [11] generators were used as the input energy source for this self-powered systems. This research area brings new challenges, especially if related to energy harvesters, which are not capable to provide sufficiently high voltage.

From the reliability aspect, investigation of the minimum requirements for self-powered systems is very important and can be handled from three points of view:

- The minimum start-up voltage at the CP input (V_{in_min}),
- The minimum start-up initial voltage at the output of a start–up circuit (V_{suc_min}),
- Self-sustaining capability,

where all three specifications are interrelated. The key challenge is to design a start-up circuit for reliable start of the whole self-powered system. There have been several techniques based on an external voltage or auxiliary voltage published so far. In [12,13], the external voltage source was used to start-up the self-powered system. Nevertheless, for battery-free systems, it is not possible to use auxiliary voltage and therefore, the start-up mechanism has to be provided in a different way. Start-up boost converter based on a vibration mechanical switch and transformer has been used in [14] and [15,16], respectively. The fully on-chip start-up techniques are presented in [17,18]. The start-up DC-DC converter based on a capacitor pass-on scheme with PMOS super cut-off technique was used in [17]. In [18], a forward body-biasing CP was employed to ensure the sufficient start-up voltage.

The paper is organized as follows. Related works focused on low-voltage driver topologies are analyzed and described in Section 3. The proposed boosted driver solution is described in Section 4. Section 5 briefly describes application of the proposed boosted driver in the self-powered CP system. The measurement setup for investigation of the reliable system start-up is described in Section 6. In Section 7, achieved results are presented and discussed. Finally, the presented work is summarized in Section 8, where also the further research aims are stated.

3. Related work

The selection of the driver topology strictly depends on the target application, i.e. digital or analog, which determines the capacitance type - parasitic capacitances or high load capacitance. In the case of digital circuits, there exist many solutions like low/high voltage swing [19,20], many kinds of adiabatic [21], pre–charged drivers [22], and so on. In this paper, digital applications are not the target ones since charge pumps are not typically implemented in such systems. In opposite, the paper deals with a boosted inverter-based driver that is suitable for high load capacitance (analog applications).
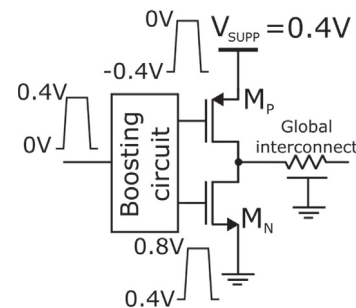
As indicated above, a driver with driving capabilities for large load capacitance needs sufficient overdrive voltage. The input voltage (transistors' V_{GS}) of the driver can be boosted using a bootstrapping subcircuit to effectively perform within low-voltage constraints. In this way, the inverter drive current can be increased multiple times, while the operation of transistors is moved up from the constrained sub-threshold regime. The boosting technique can increase the speed of driver circuits also under low power supply conditions. This in turn enhances the mixed-signal system, while the driver itself is one of the limiting blocks [23] from the performance point of view. For the sake of article consistency, the two most competitive designs are briefly described.

Paper [24] presents a driver for up-threshold circuits using capacitive boosting. Similar principle was used also in [2] with MOS transistors working in the sub-threshold regime. The last design was developed for high-speed operation and compensation of the interconnect parasitic capacitance. The main principle is illustrated in Fig. 2. The input signal of 0.4 V is boosted to 0.8 V and −0.4 V for the NMOS driver and the PMOS driver, respectively, using the internal gate capacitors.

It has been shown that using this technique, a driver operating in the sub-threshold region can increase the driving current 100 times with the driver boost voltage of 0.4 V [2]. This approach is also rather robust against PVT variations because the driver transistors are brought to the strong inversion, where the current is less sensitive to changes of V_{GS}. In this way, the propagation delay and speed of the driver are more stable over the PVT variations. On the other hand, the transistor current grows less steeply in the strong inversion. Therefore, this technique is the most efficient for sub-threshold operating ICs. The improvement in drive current comes at the expense of leakage current since the gate of M_N (M_P) must be preset to 0.4 V (0 V) before the boosting starts [2]. This technique requires capacitances, which actually ensure the boosting by their regular charging and discharging. Such capacitances can be realized by the oxide capacitance of the inverter transistor. Unfortunately, the MOS capacitance reduces in the sub-threshold region, since the depletion capacitance appears in series with the oxide capacitance [2]. Therefore, relatively large capacitors are required for this approach to be applied.

The work [25] presents the design of a sub-threshold bootstrapped driver based on a CMOS inverter. The bootstrapping is based on use of a common control circuit for both inverter transistors as depicted in Fig. 3. This circuit feeds the transistors with boosted gate voltage in driving phase ($−V_{DD}$ for PMOS device and $2V_{DD}$ for NMOS). In this way, the current density is increased. In comparison to other works, the presented scheme uses fewer transistors working in the sub-threshold region, so this solution performs better under significant PVT variations. Similarly to [2], also here the improvement can be done by feeding back the output boosting signal. Thus, the reverse leakage current can be effectively suppressed and the output boosting voltage value is maintained. On the other hand, this improvement requires the use of two additional capacitors, which increases the chip area overhead. This technique is suitable for boosting the signal from the sub-