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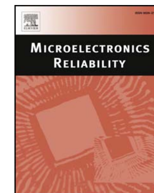

Compact modeling of dynamic trap density evolution for predicting circuit-performance aging

M. Miura-Mattausch[a,*], H. Miyamoto[a], H. Kikuchihara[a], T.K. Maiti[a], N. Rohbani[b], D. Navarro[a], H.J. Mattausch[a]

[a] Hiroshima University, Kagamiyama 1-3-1, Higashi-Hiroshima 739-8530, Japan
[b] Sharif University of Technology, Tehran, Iran

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ABSTRACT

It is shown that a compact MOSFET-aging model for circuit simulation is possible by considering the dynamic trap-density increase, which is induced during circuit operation. The dynamic trap/detrap phenomenon, which influences the switching performance, is also considered on the basis of well-known previous results. Stress-dependent hot-carrier effect and NBTI effect, origins of the device aging, are modeled during the circuit simulation for each device by integrating the substrate current as well as by determining the oxide-field change due to the trapped carriers over the individual stress-duration periods. A self-consistent solution can be obtained only by iteratively solving the Poisson equation including the dynamically changing trap density, which is achieved with negligible simulation time penalty. To enable accurate circuit-aging simulation, even for high-voltage MOSFETs, the carrier traps within the highly resistive drift region are additionally considered.

1. Introduction

Device degradation is a remaining serious problem for achieving high device and circuit performance as well as utilizing advanced technologies with ultimately scaled device dimensions. To preserve sufficient safe operating area for circuit design even after long-term usage without sufficient reduction of bias conditions, accurate prediction of circuit aging is a key. However, accurate circuit-aging prediction is still a severe task due to limitations of information about real long-term device aging as well as simulation capabilities. The microscopic electronic properties have been investigated for understanding the relationship between crystal defects and carrier trapping [1–3]. It is known that the carrier distribution in the high energy tail, the hot carriers, is an origin of the device aging [4,5]. The resulting trap-density increase due to the increased trap-site numbers is an important mechanism for the device aging in addition to inherent trap states [6,7]. The negative bias temperature instability (NBTI) effect of pMOSFETs has been a major limitation for the circuit lifetime [8,9]. Recently, the interface-state generation and the hole-trapping within the gate oxide are considered as original mechanisms for the NBTI degradation [10,11]. Therefore, compact models for circuit-aging prediction must precisely consider the carrier-trapping events during dynamic stress/relaxation repetitions according to operation-condition changes as a function of time.

Conventionally, aging is modeled as the threshold-voltage (V_{th}) shift, because aging characterization is usually done by measuring the V_{th} shift as a function of stress-bias conditions and duration [12,13]. However, the V_{th} shift alone cannot describe the complete aging effects accurately. It is known, on the other hand, that hot-carrier-induced trap-density increase is a responsible mechanism for the degradation, where the interface-trap creation is a further accompanying effect [1,2]. Therefore, detailed features of the trap-density evolution as a function of stress-bias conditions and duration must be analyzed, and the resulting findings must be considered for circuit design explicitly. Two major contributions on device aging are the hot-carrier-induced trap-density increase by the high electric field across the channel (the HC effect) [6,7] and the trap-density increase by the high electric field in the oxide (the NBTI effect) [8–11].

It is demonstrated that a surface-potential-based compact MOSFET model such as HiSIM [14], solving the Poisson equation explicitly with an iterative approach, is suitable for modeling the aging effect accurately in a self-consistent way. To model the long-term circuit aging, integration of the responsible physical quantities, such as the substrate current, is utilized to describe the trap-density increase consistently for different stress conditions. These integrated physical quantities enable description of dynamic stress-condition changes as well as dynamic trap-density increases. The long-term aging effect is also modeled with these quantities. Time constants for trapping and detrapping events determine the frequency dependence of the aging characteristics

* Corresponding author.
E-mail address: mmm@hiroshima-u.ac.jp (M. Miura-Mattausch).

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observed mostly for pMOSFETs. For aging characterization, conventional device measurements such as the *I-V* characteristics as well as the $1/f$ noise are applied. Switching measurements provide also important information for analyzing trap events. It is shown here that the long-term device aging can be modeled by the trap-density-distribution change as well [15]. Additional frequency dependence of the device-aging measurements provides further important information.

Not only modeling the trap-density evolution during the circuit operation, but also the implementation of this trap-density-evolution model into an existing compact MOSFET model is another important issue. It is verified in this context, that an iteration procedure for achieving a self-consistent compact-model solution for aging cannot be eliminated. The practical realization of circuit-aging simulation is also discussed. Some specific circuit-simulation results demonstrate, how the reported work enables the prediction of circuit aging.

2. Origin of device aging

Traditionally, the crystal quality of a Si wafer is high enough and the bias conditions applied to devices are sufficiently reduced and therefore device aging has not been a serious concern. However, device aging has recently become a serious problem due to the difficulty to reduce the supply voltage under the requirement of high circuit performances. For rather high supply voltages, carriers acquire easily energies which enable them to create additional crystal defects [6,10], resulting in additional trap states within the bandgap where carrier-trapping can occur. Therefore, to predict the device aging, the dynamic evolution of trap states and their density must be known.

There are many investigations to analyze the trap states based on different defect centers [2]. The most effort has been given to clarify the relationship between the device aging and these defect centers. Further, the time-dependent aging characteristics are sometimes complex for the NBTI effect, showing aging-feature changes according to the stress duration [16]. Fig. 1 shows trap time constants and relaxation times for energy exchange, measured at different temperatures with the time-dependent defect spectroscopy [17,18]. The different symbols refer to different trap-energy levels. Fig. 1 demonstrates that the trap events become more dynamical by increasing the temperature due to the reduced time constant values. This might induce more serious device aging at high temperature. Thus the aging characteristics can be modeled by considering the temperature-dependent trapping-time constant τ. Fig. 2 shows additionally the temperature dependence under different stress durations [19]. It is seen that long stress duration leads to different results in comparison to short stress duration. This is explained by the existence of two different components, contributing to the aging by the NBTI effect [19,20]. Modeling for circuit simulation focusses rather on long-term than on short-term stress, where high temperature results in higher device degradation with less degradation recovery.

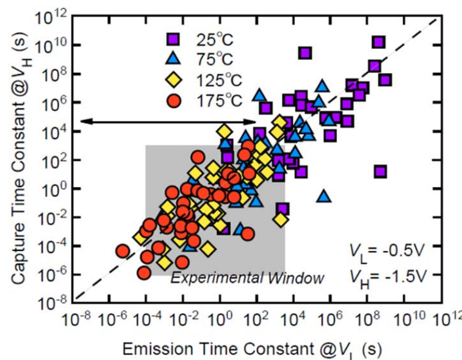

Fig. 1. Temperature dependence of trapping-time constant τ_c and detrapping-time constant τ_e. measured by the time-dependent spectroscopy [18]. The horizontal arrow shows the time scale where circuits are mostly operated.

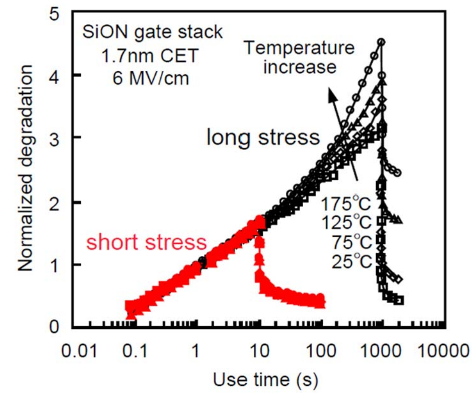

Fig. 2. NBTI stress/recovery characteristics for 1.7 nm SiON PNO gate stacks with temperature ranging from 25 °C to 175 °C. The recoverable degradation component dominates in the short-term-stress region (red symbols) while the permanent degradation component dominates in the long-term-stress region [19]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

3. Compact modeling for circuit simulation

Circuit simulation predicts the performance of circuits designed for implementation of specific functions, which are realized by combination and interconnection of many devices. Therefore the compact model, which describes the transistor characteristics as a function of bias conditions, is the key for accurate prediction of circuit performances [21]. In addition to the high accuracy, high simulation efficiency with reduced simulation time is a very important task for compact models.

Circuit simulators solve the circuit-node potentials dynamically in conjunction with the transient-current flow in neighboring devices at time t according to [22]

$$I(t) = I(V(t)) + \frac{\partial Q(V(t))}{\partial V} \tag{1}$$

where node current, voltage and charge are denoted by I, V, and Q, respectively. Thus, not only the current but also charges, induced dynamically within a device, must be modeled correctly at the same time. For this purpose, simplified analytical equations have been developed to describe device characteristics, currents as well as charges. Nevertheless, the present trend in compact modeling is to use the device-internal potential values, which are solutions of the Poisson equation, as variables to achieve an accurate description of device characteristics. This is an important improvement over the traditional compact modeling, where instead the applied bias values together with the threshold voltage V_{th} are used as model parameters. HiSIM is the first such model ever developed along this trend for more accurate compact modeling, solving the Poisson equation iteratively [23,24]. The PSP model has been developed with further approximations and without an iterative approach [25]. However, for dynamic device aging under individual stress conditions, it is difficult to describe the time-dependent trap-density evolution analytically. Additionally, no advantage in simulation time due to avoiding the iterative approach is verified. Different from 2D numerical device simulation, HiSIM solves the potential distribution in two directions independently under the approximation that the electric field along the device's vertical direction dominates in the control of the device characteristics.

As measurements, *I-V* characteristics for all nodes together with different noises properties and switching performances are available. Thus, the device-internal position dependency is not observable in circuit simulation, but rather the current flows to the nodes reflect the perturbation of carrier dynamics within the device. Individual carrier dynamics are not considered, but instead statistical features are analyzed together with the averaged carrier-energy state and physical

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