Microelectronics Reliability 80 (2018) 184–197

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Design for reliability of generic sensor interface circuits

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ARTICLE INFO

Keywords:
Sensor interface
Reliability
Reliability-aware design
Cross-layer design
Behavioral modeling
Compensation techniques

ABSTRACT

Numerous applications require the use of robust and reliable integrated circuits. In order to develop such circuits, a wide variety of influences need to be considered and also compensated if necessary. For a complete consideration of all reliability issues, the circuit has to be investigated on different levels of abstraction and together with the complete overlying system. These requirements are addressed in this work by using cross-layer design methods for the development of a generic sensor interface as an example for a complex integrated circuit. During the development, a reliability-aware design is used and major physical effects are taken into account, which alter the overall behavior of the system. Furthermore, modeling techniques are applied to port influences and circuit components from one level of abstraction to another. Possible countermeasures and compensation techniques for a reliable circuit design are also analyzed on transistor and system level. The result is a sensor interface circuit, which can be used to investigate all effects of interest and suitable countermeasures on different abstraction levels.

1. Introduction

Robust and reliable integrated circuits are required in many fields of application to ensure the failure-free operation of an overlying system for a long lifetime. This is particularly true in safety-critical systems such as automotive, aerospace or medical. For this reason, influences affecting an integrated circuit have to be taken into account during the complete design process. Typical influences are process variation and temperature dependency but also varying circuit parameters (e.g. varying supply voltage) or environmental influences like radiation. Moreover, aging is becoming a major impact in modern CMOS processes since age-dependent degradation effects such as Hot Carrier (HCI) and Bias Temperature Instability (BTI) increases for shrinking feature sizes [1,2].

In order to investigate all possible reliability issues, two points are of particular importance. Firstly, not only single transistors or circuit components have to be analyzed but the complete overlying system. Only in this way, the different impacts can be studied completely and possible interdependencies between influences and circuit components can be revealed. Secondly, a cross-level design is required since the influences need to be investigated on different levels of abstraction to meet the given specifications and to verify the complete system effectively. Nevertheless, most works on reliability are concerning only individual influences, single circuit components or do not use cross-level design methods. For example, minimizing the influence of process variations has been investigated thoroughly in the past [3]. Furthermore, methods have been proposed to conquer aging at transistor level circuit design [4,5]. Behavioral modeling has also been proposed to port reliability effects from transistor level to higher levels of abstraction and to analyze the yield of larger systems [6–8]. However, no real link between these methods has been established to develop a comprehensive cross-level design flow (Fig. 1).

Another problem can be found in modern software tools for design automation. In these tools, cross-level design techniques are not always suitable for designing complex systems. Since in most cases the same physical cause is modeled in different ways on different levels of abstraction with certain simplifications, influences are often not modeled with sufficient accuracy. Even though these models can be used for standard development tasks, problems occur while designing complex circuits for arising applications like Internet of Things, sensor cell networks, radiation hardened devices as well as Lab-on-Chip and System-on-Chip (cyber-physical systems). All of these circuits are exposed to very specific conditions that have to be taken into account at all levels of abstraction and from the very beginning of the design process.

In order to address the aforementioned problems in circuit design, this paper investigates methods for a cross-level design of a resilient system. A similar approach concerning aging effects in a continuous-time delta-sigma modulator is presented in Ref. [9]. Additionally,

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https://doi.org/10.1016/j.microrel.2017.11.029
Received 11 July 2017; Received in revised form 30 November 2017; Accepted 30 November 2017
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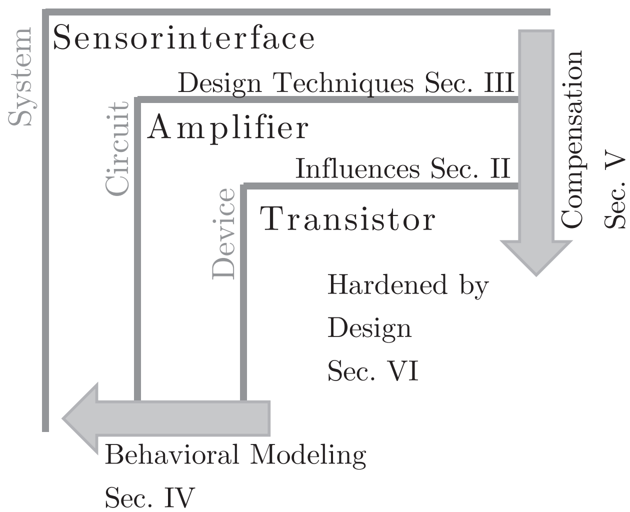

Fig. 1. Overview of the presented work.

several compensation and error correction techniques are presented in this work, which can be implemented at different levels of abstraction and increase the reliability and robustness of the system. The proposed concept of system level compensation can also be used to replace traditional compensation approaches and thus reduce the design time and costs of resilient systems. The different methods are demonstrated by using a capacitive sensor interface circuit as an example for a complex system. However, the proposed methods are not limited to capacitive interface circuits and can be applied to other interfaces (e.g. resistive, multi-sensor) as well. A sensor interface is chosen since these circuits are one of the most widely used mixed-signal systems and combine various analog and digital circuit components. In this work, it is designed to process the output signal of a capacitive sensor, which is amplified, filtered and converted into a digital output signal. The main signal path of the interface is implemented at transistor and system level to investigate it on different abstraction levels. Both circuit representations also include several non-idealities affecting the circuit behavior. Furthermore, the performance of a reliability-aware circuit design is shown exemplary by implementing the amplifiers in the main signal path of the interface.

This work is structured as follows. Section 2 gives an overview of the influences that have to be considered during the design of a system, spanning from influences concerning individual transistors up to influences concerning the whole system. Section 3 introduces approaches for reliable circuit design methods in order to conquer reliability issues at circuit level. The following Section 4 presents behavioral modeling techniques, which are used to port different effects to a higher level of abstraction and therefore enable the analyses of larger systems. In Section 5, a monitoring concept is described, which detects and corrects various influences on system level. The capacitive sensor interface, its representation at transistor and system level as well as the reliability-aware design of the utilized amplifiers is presented in Section 6. The final Section 7 concludes this paper.

2. Influences on integrated systems

Due to the evolving fields of application for electrical devices and their demanding requirements, a steadily increasing number of influences have to be taken into account during the design steps of modern integrated circuits. The most commonly mentioned influences are temperature/humidity, pressure/strain, radiation, voltage/current, process variation and time [10]. This list of **P**rocess, **V**oltage, **T**emperature, **A**ging and additional influences is hereinafter referred to as **e**xtended **ePVTA**.

Besides the pure functionality of devices, modern transistor models also contain a number of ePVTA influences. The kind of the chosen influences, which are considered within the model, usually depends on the specific modeling approach (BSIM [11], EKV [12], PSP [13] or proprietary models). Generally, process variations and aging dependent influences are considered with additional external models and simulation environments, while temperature influences are usually included in the transistor models. Transistor models are coded in hardware-oriented programming languages and are used within SPICE simulators. On this level of abstraction, the impact of fluctuations of voltages and currents can be analyzed directly. Other influences like pressure, humidity and radiation can only be analyzed by FEM simulations, which are very time consuming.

2.1. Consideration of influences

The above mentioned influences have specific impacts on transistors, circuits and systems. On each level of abstraction, another way of describing and dealing with these impacts is used. The crucial effects and their consideration on these three levels are shown in Fig. 2.

2.1.1. Transistor level

Firstly, the influences are observed, measured and modeled on the single device level since it is the only way to minimize the coincidental consideration of other effects. Subsequently, they are clustered into sections which correspond to their specific origins or repercussions. At this level, only a very few countermeasures exist for the mentioned influences. The process can be improved in order to reduce the process variation and the layout of the device can be adjusted to be robust

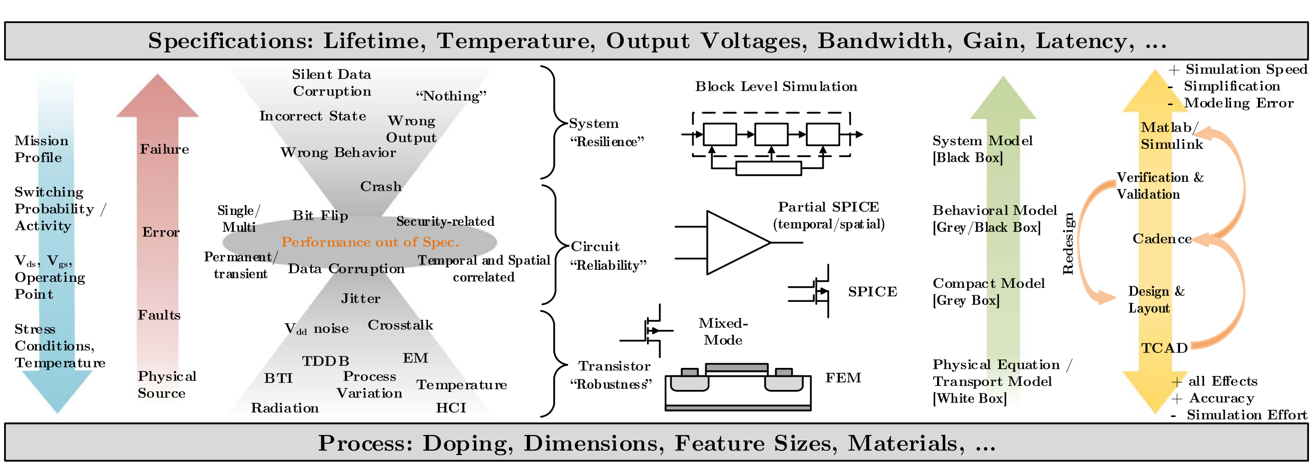

Fig. 2. Influences on integrated circuitry and their consideration and modeling at different levels of abstraction.