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Modulation method for measuring thermal impedance components of semiconductor devices

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ABSTRACT

The paper describes the modulation method of measuring the thermal impedance of semiconductor devices as well as its implementation. In contrast to the standard method (JESD51-1 standard) which requires heating the device under test by the stepped power, the modulation method uses heating power modulated harmonically. A pulse sequence of heating current, with the pulse length varying harmonically, is passed through the device under test. The p-n junction temperature is measured through a temperature-sensitive parameter, namely a forward voltage drop on the p-n junction between heating pulses at low measuring current. First harmonic of the p-n junction temperature oscillation is determined by the discrete Fourier transform, which allows to determine thermal impedance absolute value and phase at modulation frequency of heating power. An analysis of the dependence of thermal impedance on modulation frequency allows to determine thermal impedance components corresponding to the structural elements of the device under test. Numerical simulation shows that the thermal resistance components on the Foster's network may be determined at the modulation frequencies corresponding to the first derivative minima of the thermal impedance of the real part of frequency dependence. The main characteristics of the device that implements the method are described.

1. Introduction

According to JESD51-1 [1], thermal resistance R_{Tjx} relative to the case or environment of semiconductor devices is defined as follows:

$$R_{Tjx} = \frac{T_j - T_x}{P} = \frac{\Delta T_j}{P}$$

where T_J = device junction temperature in a steady state test condition;

T_X = reference temperature of the case or environment;

P = dissipated power.

The p-n junction temperature T_j is measured indirectly by looking at some temperature-sensitive parameter (TSP). For example, JESD51-1 uses forward voltage drop at low measuring current as TSP. For LEDs, it is possible to use the peak wavelength [2], for high power MOSFETs, source-drain forward voltage or drain-source on-resistance can be used [3], for IGBT, collector-emitter voltage can be used [4]. In most cases, according to standard JESD51-1, the forward voltage drop at low measuring current is used as TSP.

High power MOSFETs and IGBT-transistors are the most interesting measurement objects because they are able to switch hundreds-ampere currents and their dissipating power can be up to 1 kW. Such operating modes can cause dramatic overheating of the transistor's chip with subsequent negative effects. Thermal resistance measurement is especially important for high power LEDs and devices based on them because high dissipated power can cause a dramatic reduction of the quantum yield and even cause the device destruction [5]. The efficiency of heat removal from a LED's p-n-junction to the heat sink and then to the environment depends on a LED's construction (Fig. 1). Moreover, each element of the LED has its own thermal resistance. For manufacturers of powerful LEDs and LED based devices it is necessary to estimate thermal resistance values for every construction element in order to minimize “junction to case” thermal resistance.

To solve this problem and to determine temperature distribution in LED construction, thermal models based on the principle of thermal-electrical analogy are usually used. According to this principle thermal flow processes (“p-n-junction – substrate – thermal pad – PCB – heat sink”) are similar to electrical processes in equivalent electrical circuit (Fig. 2), which is a set of sequentially connected RC-chains. Electric current in the equivalent circuit corresponds to thermal flow through the construction elements, voltage corresponds to temperature. Every RC-chain corresponds to its LED's construction element or construction

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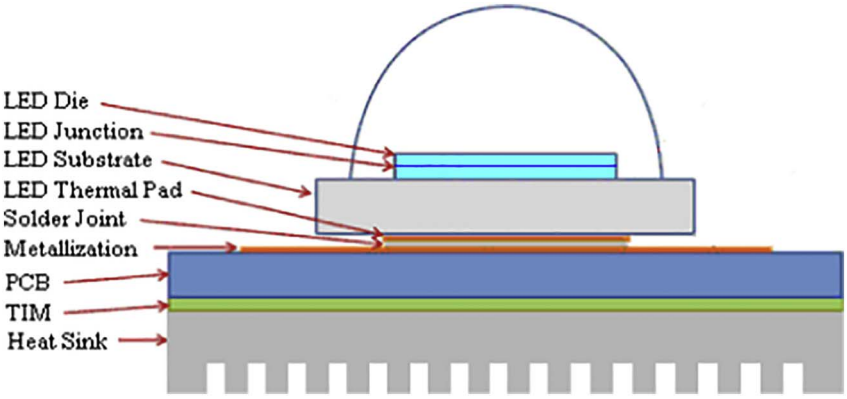

Fig. 1. Graphical representation of the thermal path between junction and case and junction and solder pad [6].

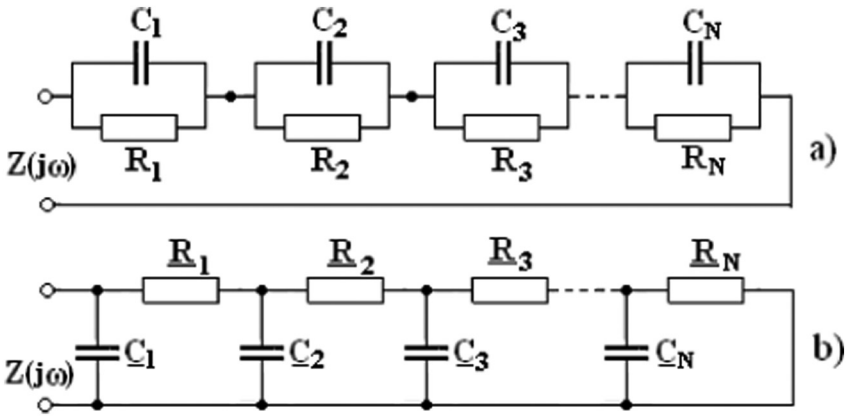

Fig. 2. Canonical models for RC one-ports. a) FOSTER network, b) CAUER network.

layer. Electric resistance of the RC-chain is a counterpart of thermal resistance, electric capacity is a counterpart of heat capacity, chain's constant time $\tau = R \cdot C$ is a counterpart of thermal time constant of a construction element.

Determining thermal resistance components may be based on both Foster's network and the Cauer's network. Parameters of each network are different, but it is possible to convert parameters of Forster's to Cauer's network. Procedure of such conversion is represented in the JESD51-14 standard [7].

2. Standard method of thermal resistance measurement

The idea of determining the thermal resistance components is based on the analysis of the heating curve (rising curve of junction temperature $\Delta T_j(t)$ while device under test (DUT) is heated by known heating power P_H) or cooling curve (decrease of junction temperature after heating the DUT to the state of thermal equilibrium).

Heating curve can be obtained by dynamic test method under JESD51-1 standard by heating the DUT with heating pulses with variable length t_H, measuring the heating power in the time of heating and measuring voltage temperature coefficient VTC before and after heating.

Analytically, increment of junction temperature by heating with a known heating power P_H for a linear thermal model can be expressed by eq. [8]:

$$\Delta T_j(t) = T_j(t) - T_j(0) = \int_0^t h(t-t')P_H(t')dt' = P_H \int_0^t h(t-t')dt'$$

where $T_j(0)$ – initial junction temperature, $h(t-t') = \sum_{i=1}^{m} \frac{R_{Ti}}{\tau_{Ti}} \exp\left(\frac{t-t'}{\tau_{Ti}}\right)$ – function of the circuit response to a δ-impulse at the time t', which is determined by the thermal network parameters.

Typical shape of the heating curve is shown in Fig. 3a [1]. If a logarithmic time scale is used, it's easy to see areas of slow and fast thermal response changes that correspond to the layers of the structure of the measurement object. The section of slow change (flat part of the curve) corresponds to the heat accumulation in the particular layer; the part of the curve that represents rapid change corresponds to the heat flux reaching the next layer. In this way, heating curve carries information about the contribution of several construction parts to the overall thermal resistance. The example of such could be the following layers: die - substrate - case - printed circuit board (PCB) – heat sink – environment.

JESD51-14 [8] describes the method for measuring the cooling curve of the DUT. It measures the junction temperature by thermal sensitive parameter after heating power is switched off while heating the DUT to a steady thermal state. As noted in [7], strictly speaking, the heating and cooling curves are somewhat different, but in the linear thermal model approximation they are quite close and in the redistribution of the approximation error the cooling curve will repeat the heating curve with the opposite sign.

A method based on structure function, which was first proposed in [7] and developed in [9,10], is used to get information on the contribution of individual units of a thermal model to the overall thermal resistance. According to this method, a thermal model of the measurement object is described by Cauer's network (Fig. 2) and structure function $K(R_{T\Sigma})$ is used to determine the components of thermal resistance:

$$K(R_{T\Sigma}) = \frac{dC_{T\Sigma}}{dR_{T\Sigma}},$$

where total heat capacity $C_{T\Sigma}$ on total thermal resistance $R_{T\Sigma}$ that are defined as follows:

$$C_{T\Sigma} = \frac{P_0 \cdot t}{T_j(t) - T_j(0)}, \qquad R_{T\Sigma} = \frac{T_j(t) - T_j(0)}{P_0}.$$