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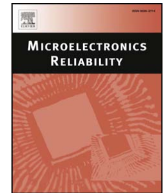
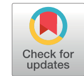


Reliability and failure analysis of SAC 105 and SAC 1205N lead-free solder alloys during drop test events



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ABSTRACT

The purpose of this study is to establish a predictive fatigue life model for SAC 105 (Sn-1.0Ag-0.5Cu) and SAC 1205N (Sn-1.2Ag-0.5Cu with nickel) lead-free solder alloys. A simulation model approach was developed to investigate the stress and strain of the solder joint during drop tests. A Joint Electronic Device Engineering Council (JEDEC) Condition B drop test was simulated. This test is characterized by a 1500*g* peak acceleration for an impulse duration of 0.5 ms. At the point of impact during the drop test, the deformation of the printed circuit board (PCB) via bending and mechanical shocks can cause joint cracks in the solder. To establish a predictive model for the 10% fatigue life of the lead-free solder joint under drop test conditions, the study was conducted in three main phases: material analysis of the lead-free solder alloy, the drop test model, and the 10% fatigue life analysis. Tensile tests of SAC 105 and SAC 1205N were used to examine the elastic and plastic behavior of the solder alloy mechanism. Simulations and drop tests were performed to investigate the failure of the microelectronic package resulting from the drop test. The predictive fatigue life models of SAC 105 and SAC 1205N were validated by the experimental results with satisfactory accuracy.

1. Introduction

Portable microelectronic devices have become lighter and thinner, allowing them to be easily carried; however, these devices can be accidentally dropped on the ground, resulting in damage to the device. To improve the reliability of portable microelectronic devices, a drop test standard has previously been formulated; in 2003, Joint Electronic Device Engineering Council (JEDEC) Solid State Association published board-level drop test standards for both industry and academia [1]. The present study adopted condition B of the JEDEC standards, which states that the tested product is to be dropped under half-sinusoidal acceleration with a time-dependent peak acceleration of 1500*g* for an impulse period of 0.5 ms. As a part of the test, the test board is to be fixed on the drop table. Next, the table is dropped onto the shock generator via freefall from the required height. Both simulations and experiments are used to investigate the failure of the microelectronic package resulting from the drop test.

To mitigate shortcomings in the standard, Tee et al. [2–6], Luan et al. [7–10], and Goh et al. [11] developed the Input G method, which can be incorporated into the simulation models. In this approach, the acceleration sensor is installed near the screw hole, allowing the acceleration history to be measured and recorded. This approach allows the simulation model to omit components of the drop table itself, such as screws and other structures, thus substantially reducing the computing time. The simulation results obtained using this method are more accurate and more widely applicable than those of the model that accounts for all elements in freefall. Chou et al. [12,13] performed a drop test simulation to investigate the stress and strain of solder joints of the filling materials and dielectric layers of wafer-type packages and to determine a method to design the copper trace layout to suppress cracks in the copper traces. The Support Excitation Scheme method was proposed by Yeh et al. [14,15] and applied by others [16–19]. Unlike the Input G method, the drop test loading uses a body force applied to the drop test model. Most previous studies have used finite-element modeling to analyze the stress, strain, and deformation of solder joints during drop tests. Other researchers have suggested investigating the cross-section of solder joints through experimental drop tests. To investigate the plastic deformation of solder joints, a digital image correlation (DIC) technique was used [20]. The solder joint microstructure and its orientation at different cooling rates on the printed circuit board (PCB) assembly was observed using orientation imaging microscopy [21]. An analytical predictive model was proposed for evaluating the dynamic stress of solder joints in ball grid array (BGA) and column grid array (CGA) packages [22]. According to [23], the majority of functional failures, such as wire bond fracture, solder fracture, and die attach delamination, in the tested MEMS components were caused by

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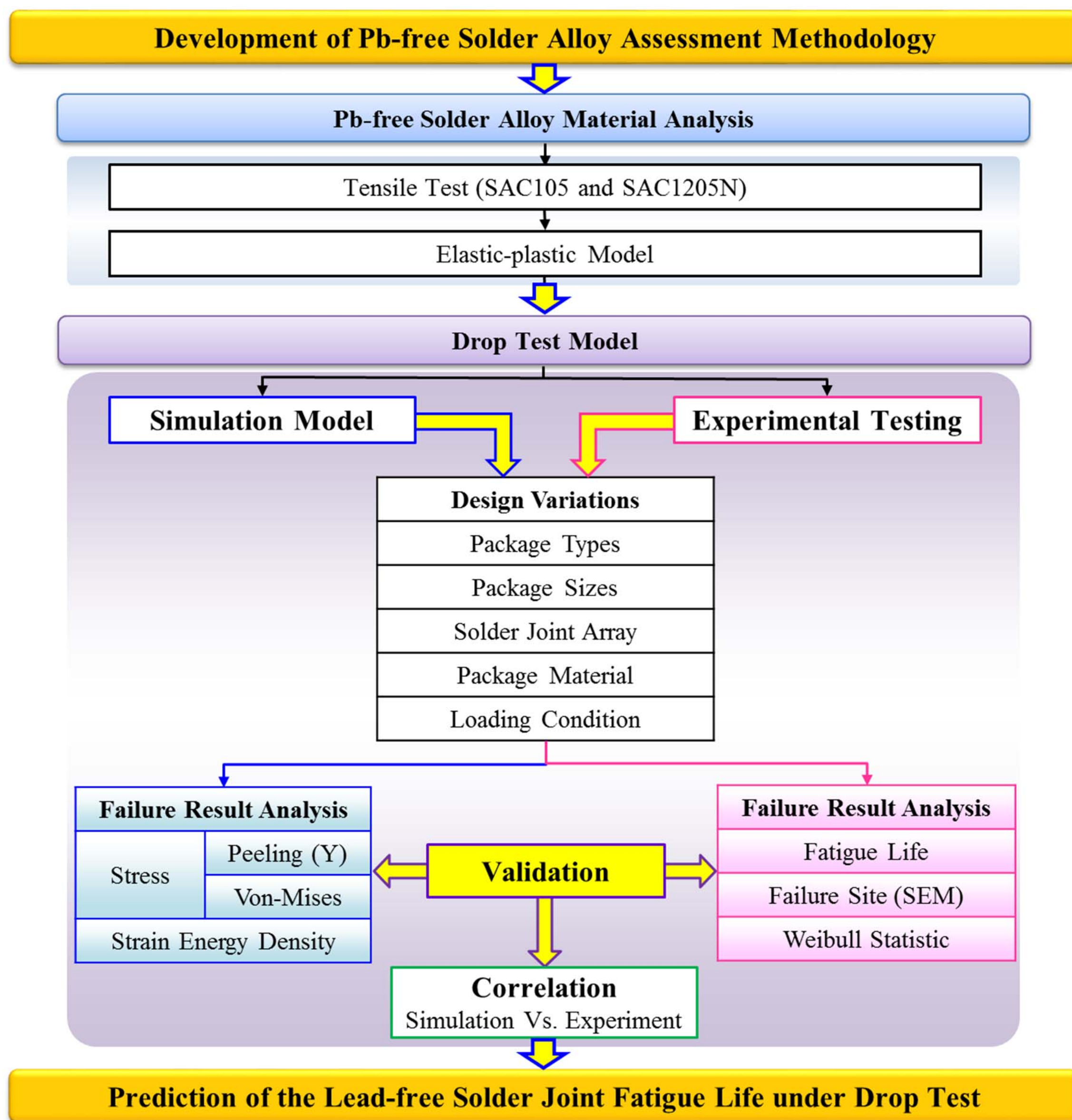

Fig. 1. The flowchart of the research.

failure sites in the MEMS package. Pearl et al. [24] investigated the mechanical reliability of solder interconnects formed on ENEPIG and immersion silver surface finishes subjected to drop loading reliability tests. Furthermore, a description of the printed circuit board and the drop loading reliability test procedure was provided, and the results of the test and analysis of the failures were presented. During the drop test, the solder joint was deformed, and a fracture was induced by the bending of the PCB. The bending is the primary structural response of the board-level drop test. The PCB bending not only caused the failure of the solder joint but also resulted in the fracturing of the die and die attach. Ren et al. [25,26] and Jia et al. [27] conducted three-point bending tests of package-on-package scenarios and examined the fractures of die and die attach. The results revealed that the crack initiation behavior and the crack defect and bridge propagation behavior were affected by the die attach layer.

We provide a brief description of a computerized physics of failure (PoF) approach that is designed to evaluate the life expectancy of microelectronic assemblies. A case study demonstrating this approach is also provided. Life expectancy estimations of microelectronic products assist equipment manufacturers in determining warranty periods, maintenance schedules, and repair and replacement times. In addition, products are required to meet the reliability and life-cycle requirements that customers have come to expect. Because of increasing competition and technological obsolescence, equipment manufacturers are required to reduce the time-to-market of new products in a cost-effective manner. Traditional methods of product qualification that involve expensive and time-consuming physical tests can be replaced by computer simulations that replicate the physical tests. These simulation programs must take into consideration the responses of a product under the anticipated use and test conditions. Based on the responses, the failure sites and mechanisms should be identified, and the time to failure should be estimated. The failure sites and mechanisms in microelectronic assemblies and commonly used PoF models are briefly discussed herein.

The product life is correlated to the stress and strain developed in microelectronic assemblies under loading conditions, such as drops, shocks, vibration and thermal, mechanical, chemical, and electrical disturbances. The stress and strain developed in the interconnections in microelectronic assemblies can be evaluated using general-purpose computer simulation software, such as ANSYS software. Such

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