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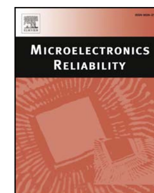

Test response compaction method with improved detection and diagnostic abilities

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ABSTRACT

This paper describes a test response compaction method that preserves diagnostic information and enables performing a test-per-clock offline test. The test response compaction system is based on a chain of T flip-flops. The T flip-flop signature chain can preserve the information about the positions of the erroneous test response occurrence and the information about the clock cycle when the erroneous test responses occurred. This information can be used for diagnostic purposes. An algorithm that localizes errors according to the T flip-flop chain output is presented. The paper discusses the possible benefits and limitations of the proposed test pattern compaction scheme. The influence of multiple errors on detection and localization capability of the compaction system and hardware overhead is discussed in the paper as well. The probability of error masking is analyzed, the proposed scheme provides substantially lower masking probability than a D flip-flop chain and a MISR. The scheme can spare the test time by the test-per-clock arrangement. The hardware overhead and reached test time are given for several benchmark circuits in the paper as well.

1. Introduction

Diagnosis at system level become challenging for nowadays embedded devices. The information about the hardware structure is not usually available, and it's hard to distinguish the root cause of a failure. Built-In Self Test (BIST) of the random logic is often used in testing as it is applied to isolated components and the test result can be processed at the system level. BIST can provide more detailed diagnostic information than the go/no-go bit. The deeper knowledge can be advantageously used for manufacture improvements and in field maintenance.

Embedded cores can be advantageously tested by mixed mode testing methods [5,6,16,18]. These methods either use a given number (say 10,000) of pseudo-random test vectors followed by deterministic test vectors detecting random resistant faults or they use pseudo-random patterns with several care bits fully defined. All these vectors have to be serially shifted test by test into several parallel scan chains. This mechanism causes long test session time and a big amount of energy consumed for testing. The main reason of long test application time is the necessity of manifold reloading of test patterns into the scan chains through a narrow Test Access Mechanism. This problem is partially solved in RESPIN, or RESPIN + + architecture [19] where the test patterns are decompressed within inner cores of the SOC circuit and the core under test (CUT) scan chains can be loaded in parallel with higher clock frequencies. Another possibility is to transfer compressed test vectors to the tested circuit and decompress them on a chip [18,12]. Nevertheless, the total test time for complex circuits remains relatively long, and the total energy consumption for the test is quite high due to the vast number of performed shifts. The test time can be shortened by avoiding the clock cycles that have to be generated in order to shift the test patterns in and test responses out from the CUT.

The complete diagnostic test consists of many times higher number of the test pattern and test response transfers through the Test Access Mechanism. There are two basic techniques used for random logic BIST diagnostics. The first one uses unmodified standard architecture. The test is composed of several test sessions that narrow down the number of fault candidates. The test sessions are repeated many times with different parameters [2,21,3,13]. This type of diagnostic testing is time-consuming and requires using a special tester. The second technique uses a special hardware for storing the erroneous test responses that can be downloaded at system level [4,1]. The diagnostic information can be extracted from the stored error signatures. Embedded test processor and an adder are used for compaction, de-compaction, and comparison of test response samples with real test responses [8]. This hardware spares memory and time for diagnosis.

A significant problem of reduced error detection rate arises if the test responses contain unknown responses (so-called X values) [10]. Simply using a standard multiple input signature register (MISR) for multi-scan chain response compression causes that the test responses

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are mixed together, and the tester has to ignore all signature bits with unknown values. There exist several approaches eliminating or reducing the X values influence. It is possible to mask the X values before they enter the compaction hardware [20]. This could be relatively hardware consuming. Another possibility is to use such compactors that reduce the error masking probability. In [17] compactors based on error correcting linear codes are proposed. The error bits are determined with the help of post processing at the tester. In [10] each scan chain output is connected to several 1-bit compactors in such a way that the X values cannot simultaneously mask all the connected compactors. This arrangement detects all single errors. In [9,7], a scheme that accelerates the fault diagnosis was used. The proposed solution uses a feedforward DFF shift registers instead of the MISRs with a feedback tap. The register is fed from the parallel scan chains, and the clocking frequency of the scan chains and the register is lower than the frequency of shifting out the register content. The transfer of the signature to the tester is performed with the reduced incidence. Reading of all test responses with the exception of the X values can be guaranteed with the help of the appropriate timing the sampling points.

In [11] so-called convolutional compactors were introduced. They use XOR networks designed according to selected characteristic polynomials that guarantee to preserve the diagnostic information. In [14], we proposed a similar test response compaction system with improved error detection and diagnostic capabilities based on using simple feedforward T flip-flop signature analyzer (SA) instead. This approach differs from [11] in the possibility of joining the detection and diagnosis test phase into one, and it reduces the number of clock cycles devoted to diagnosis. In this article, we refine the research results and quantify the diagnostic ability of the proposed system.

Scan-based testing can be extremely time-consuming. If there were a possibility of efficient test pattern loading and output response preserving during the test session, it would speed up testing substantially. This can be achieved with the test-per-clock methods [15]. In [14] we combined test-per-clock testing approach with the test pattern overlapping method [16] which provided us shorter test sessions.

The paper is organized as follows: In Section 2 we introduce the T flip-flop (TFF) based SA, discuss the fault detection capabilities, quantify the fault-diagnosis ability, propose the fault localization algorithm and compare the results with the DFF solution. In Section 3 we discuss the resistivity against X values. In Section 4 we propose the test-per-clock test access mechanism using the TFF response compaction, and we estimate the hardware overhead requirements. Section 5 concludes the paper.

2. T flip-flop signature analyzer

Let us consider to have multi-scan chain design with a signature register (MISR). This mechanism creates a hash of all bits shifted through the chains. Linear feedback shift register (LFSR) [17] or a DFF shift register with no feedback tap [7] is usually used as a MISR. We propose to use a TFF chain with no feedback tap replacing the original MISR. This solution spares the feedback and has a lower probability of error aliasing than the DFF shift register. As the TFF is not usually included in technological libraries, we can create it by adding a local feedback added to the DFF as it is shown in Fig. 1. A TFF stores the odd parity bit of the data stream that is fed into its input which means that it can detect every bit flipping on its input.

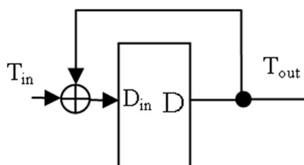

Fig. 1. TFF scheme.

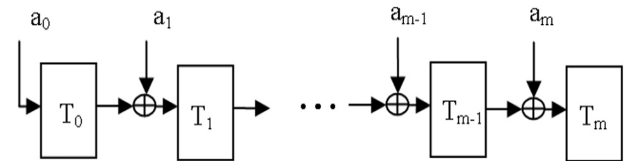

Fig. 2. The TFF based (m + 1)-input SA.

If we concatenate a set of TFFs into a TFF chain according to Fig. 2, the formed SA will store and distribute the parity information of it's all parallel input bit sequences. In this paper, we suppose that a multi-scan chain response compression is used which means that the TFF register is loaded by the scan chain outputs. TFF register can be effectively used for error signature preservation as the information about errors is stored not only in the TFF that detected the error, but it is diffused to the TFFs at the right-hand side of the error registering TFF. The TFF chain has one more advantage comparing with the standard LFSR: The clock cycle and the TFF into which an error enters can be calculated easily as the register has no global feedback that mixes the captured responses according to the generator polynomial. From this reason, we are able to describe the TFF chain by a simple regular graph that represents spreading the information about the erroneous input bit through the chain.

2.1. Error detection

Let us have $(m + 1)$ parallel scan chain outputs feeding a $(m + 1)$ bit TFF chain (Fig. 2). We consider that the current state of the TFF chain is $x_0^0, x_1^0, \ldots, x_{m-1}^0, x_m^0$ and the test responses on the scan chain outputs are $a_0^0, a_1^0, \ldots, a_{m-1}^0, a_m^0$. After the ith scan chain clock cycle, the scan chain output bits will be $a_0^i, a_1^i, \ldots, a_{m-1}^i, a_m^i$. After performing several clock cycles, we obtain a new TFF chain states that are shown in Table 1.

There are several possibilities how to represent the TFF chain error detection capabilities. We have chosen a colored graph as it gives an immediate information about error detection (black color) and no error detection (white color). Fig. 3 represent three cases of error propagation through the TFF chain. The first one accounts for a single error propagation the next two a double-error propagation. Fig. 3 consists of 17 columns and 36 rows. Each row corresponds to one clock cycle; each column corresponds to a sequence of states of one TFF. The black squares represent the TFF positions and clock cycles where the logical value is flipped due to the error. The rightmost unflipped bits are colored by yellow color in order to highlight the TFF chain output SO. If we are interested in such an error that was introduced into the TFF chain for example in the 0th TFF during the clock cycle 0, the black colored squares indicate the relative TFF position and the clock cycle where and when the value of TFF was flipped.

Let us have a look in more detail at the graph. The erroneous logical value was introduced into the 0th TFF and 0th clock cycle (the (0,0)-square in the figure has the black color, it is the root of the error graph). During the next clock cycle, the erroneous logical value is preserved and simultaneously diffused to the nearest right neighboring TFF (the corresponding two squares in the next row are black). After the 16th clock cycle, the square on the (*16*,*16*)-square is black together with several interlacing squares. We can see that if the distance between the TFF, where an error occurs, and the SO is shorter or equal than the number of performed clock cycles, the error is detected by the TFF output SO (the rightmost column of the figure). For each error position, we can find a column that corresponds to the erroneous SO sequence (depending on the TFF chain length). It could be of reader's interest that the graph in Fig. 3 has the same shape as the Sierpinski gasket. The second and third graphs represent two different double-error graphs. The positions and clock cycles in which the errors enter the TFF are marked by an error bubble.

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