Microelectronics Reliability 80 (2018) 257–265

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Invited paper

Positive and negative threshold voltage instabilities in GaN-based transistors

G. Meneghesso, M. Meneghini*, C. De Santi, M. Ruzzarin, E. Zanoni

University of Padova, Department of Information Engineering, via Gradenigo 6/B, 35131 Padova, Italy

ARTICLE INFO

Keywords:
GaN
Transistor
NBTI
PBTI
Degradation
HEMT

ABSTRACT

This paper reviews the main mechanisms responsible for bias-temperature instability (BTI) in GaN-based high electron mobility transistors. In the first part of the article, we focus on the threshold voltage instabilities of GaN-based MIS-HEMTs submitted to positive and negative gate bias. We demonstrate that the shift in threshold voltage originates from the trapping/de-trapping of defects located at the insulator/semiconductor interface and/or in the bulk dielectric. In the second part of the paper, we describe the threshold voltage instabilities of GaN-transistors with p-GaN gate, designed specifically for normally-off operation. We present original data indicating that under positive gate bias these devices with p-GaN gate may show a negative threshold voltage shift, which is fully recoverable. This effect is ascribed to the injection of holes under the gate contact, and to the corresponding accumulation of positive charge, possibly at the p-GaN/AlGaN interface.

The results described within this paper provide an up-to-date description of the most relevant trapping processes that impact on the stability of threshold voltage and on-resistance in GaN-based transistors.

1. Introduction

Energy efficiency is one of the global challenges of the 21st century: typically, power converters have efficiencies in the range 85–95%, depending on the power and frequency level. As a consequence, at global level, nearly 10% of the global electricity is wasted in conversion losses, and this corresponds roughly to the total amount of generated renewable energy. The core of a switching mode power converter is the transistor (switch), which is typically made of silicon. To reduce the conversion losses in the power converter, the resistive and switching losses of the transistors must be minimized. Silicon has served the power electronics field for years, and is currently covering the largest share of the power electronics market. However, due to intrinsic material limitations, silicon is not the best material for the fabrication of "zero-loss" switches, and other materials are currently under investigation, including SiC, GaN and Ga_2O_3. Among these, gallium nitride is demonstrating excellent properties for application in power conversion: the wide bandgap (3.4 eV [1]) permits to reach high operating temperatures (> 300 °C, [2]), thus reducing the need of large size heat sinks and/or liquid cooling; the high electron mobility permits to reach very low values of the on-resistance (< 25 mΩ for 60 A/650 V devices, [3]), thus minimizing the resistive losses of the devices. Finally, the low gate charge * on-resistance product ($R_{on} * Q_g$, < 1 nC*Ω) leads to significantly lower switching losses. Thanks to these advantages, power converters with efficiency in excess of 99% have already been demonstrated, [4].

One of the biggest issues of GaN-based devices is the stability of the main parameters (threshold voltage, V_{th}, on-resistance, R_{on}) during operation. Several papers (see for instance [5–9], [10–12]) indicated that charge trapping processes may significantly affect device performance. When exposed to off-state conditions, the on-resistance may significantly increase due to charge trapping at the surface [13], in the buffer [14,15,16] and under the gate [6,9]. Threshold voltage instabilities have been demonstrated both under positive [6,9] and negative gate bias [10–12], [17], due to the presence of traps in the gate insulator (for insulated-gate devices, [18]) or under the gate (for transistors with p-GaN gate, [19]).

The aim of this paper is to present an overview of the main trapping processes responsible for bias-temperature instability (BTI) in GaN-based HEMTs. We discuss our recent data on the topic, and compare them critically with recent papers in the literature. The paper is divided in two parts. The first part is focused of metal-insulator-semiconductor (MIS) high-electron mobility transistors (HEMTs). We present results on the positive threshold voltage shift induced by the exposure to positive gate bias and on the negative threshold voltage shift induced by operation under negative gate bias. We demonstrate that under positive gate bias there exists a correlation between the current injected from the gate and the overall threshold voltage shift, indicating that trapping is favored by the gate leakage current, which promotes the filling of defects located at the interface between the dielectric and the semiconductor and in the dielectric. In addition, we show that under negative gate bias, a negative threshold voltage shift is observed in GaN-

* Corresponding author.
E-mail address: matteo.meneghini@dei.unipd.it (M. Meneghini).

https://doi.org/10.1016/j.microrel.2017.11.004
Received 28 July 2017; Received in revised form 6 November 2017; Accepted 8 November 2017
Available online 20 November 2017

based MIS-HEMTs. This is ascribed to the de-trapping of defects at the AlGaN/insulator interface. Both processes are recoverable, with different (and non-exponential) kinetics.

The second part of the paper is centered on the analysis of the threshold voltage instabilities of normally-off transistors with p-type gate. We demonstrate that these devices may show a negative threshold voltage shift when they are subjected to positive gate bias (this is contrary to what observed in MIS-HEMTs where typically a positive gate bias leads to a positive threshold voltage shift). This effect, that leads to a slight increase in drain current, is ascribed to the trapping of positive charge, possibly at the p-GaN/AlGaN interface, which can be promoted by the injection of holes from the gate.

2. Experimental details

The analysis presented within this paper was carried out on two kinds of devices. The first part of the study, focused on MIS-HEMTs, was carried out on D-mode MIS-HEMTs grown on a Si substrate. The epitaxial structure is constituted by an AlN nucleation layer, a 2.3 µm AlGaN buffer layer, a 150 nm GaN channel layer, an AlGaN barrier (which is recessed to 3.7 nm under the gate) and a 15 nm SiN gate insulator (see Fig. 1). Details on the structure can be found in [20]. These devices were subjected to positive-gate pulsed measurements, with the aim of investigating the dynamic modifications in the threshold voltage induced by the exposure to a positive gate voltage. dc testing was also carried out, with the aim of studying the correlation between gate leakage current and the overall threshold voltage shift under positive gate voltage. The same set of samples was also subjected to negative gate stress, with the aim of studying the NBTI. Threshold transient measurements were carried out with the aim of describing the kinetics of threshold voltage modifications and the related temperature dependence. A specific setup allowing to monitor the threshold voltage variations over stress time was developed to this aim. In most cases [10], threshold voltage instabilities are studied by using high-temperature gate bias (HTGB) or high-temperature reverse bias (HTRB) conditions. We propose a further operating condition (high temperature source current, HTSC) to study the impact of semi-on state regime on the threshold voltage [11]. The devices are subjected to stress at high drain bias, while pulling a low current out of the source. This process promotes the trapping of hot-electrons, thus leading to a different behavior with respect to what is observed in off-state (HTRB) conditions.

In the second part of the paper, we report results obtained on commercial normally-off devices with p-type gate. On these, we carried out constant-voltage stress tests, with the aim of describing the variations in threshold voltage induced by positive gate stress. The analyzed devices feature a threshold voltage higher than 1 V, and have subjected to step-stress at positive voltages up to 10 V, to describe the recoverable and permanent degradation processes and discuss the related physical origin.

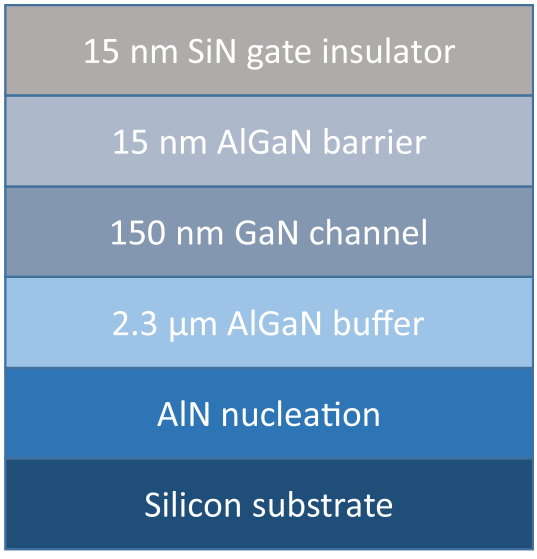

Fig. 1. Schematic structure of the described devices (see details in [10]).

3. PBTI and NBTI in MIS-HEMTs

3.1. Positive threshold voltage instability

Recent studies [5–7], [9], [21] indicated that GaN-based MIS-HEMTs may suffer from positive and negative threshold voltage instability when subjected to stress under positive/negative gate bias. In order to address this issue, we developed a specific approach, based on the use of combined pulsed measurements and constant voltage stress tests. Pulsed measurements are closer to real operating conditions, when devices are repeatedly switched on and off. On the other hand, constant voltage stress tests induce a more severe degradation of device characteristics, since the device is continuously exposed to the stress bias; constant voltage experiments are of fundamental importance, since they allow one to extrapolate the kinetics of the variation of the main device parameters (V_{th}, R_{on}), and to formulate hypothesis on the possible degradation processes.

Fig. 2 reports the pulsed I_D-V_{GS} curves measured on a MIS-HEMT after exposure to stress at negative and positive quiescent bias. The measurement procedure is as follows: the devices are kept at a quiescent gate bias (V_{GS_Q}). Every 100 µs, the quiescent bias is quickly (1 µs) removed, to measure one point of the I_D-V_{GS} curves. Since - as described below - the de-trapping kinetics are very slow, during the 1 µs on-state phase, the device does not have time to recover, and the impact of charge trapping is maximized. For these measurements, the quiescent bias on the drain was kept at zero (during stress only), while the quiescent bias on the gate was changed from − 6 V to + 5 V. Fig. 3 summarizes the results in Fig. 2, by reporting the variation of threshold voltage as a function of the quiescent bias applied to the gate. As can be noticed, the exposure to a negative gate bias induces a small negative shift in threshold voltage (− 0.5 V at V_{GSQ} = − 6 V, see Fig. 3); on the other hand, a relevant shift in threshold voltage is observed under positive gate bias (+ 3 V at V_{GSQ} = + 5 V, see Fig. 3).

The presence of positive and negative threshold instability can be

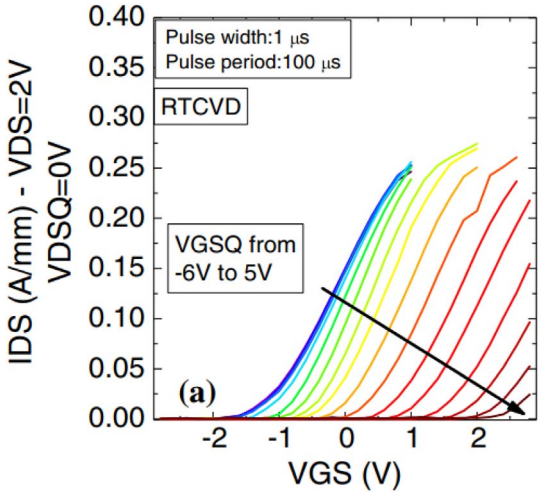

Fig. 2. Pulsed I_D-V_{GS} measurements taken on a MIS-HEMT after inducing trapping with different quiescent gate voltages, from − 6 V to 5 V. Reprinted from Microelectronics Reliability, 55, I. Rossetto, M. Meneghini, D. Bisi, A. Barbato, M. Van Hove, D. Marcon, T.-L. Wu, S. Decoutere, G. Meneghesso, E. Zanoni, "Impact of gate insulator on the dc and dynamic performance of AlGaN/GaN MIS-HEMTs", Microelectronics Reliability 55 (Copyright 2015) 1692–1696 with permission of Elsevier [20].