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Border traps and bias-temperature instabilities in MOS devices☆

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ABSTRACT

An overview of the effects of border traps on device performance and reliability is presented for Si, Ge, SiGe, InGaAs, SiC, GaN, and carbon-based MOS devices that are subjected to bias-temperature stress, with or without exposure to ionizing radiation. Effective border-trap densities and/or energy distributions are estimated using capacitance-voltage hysteresis, low-frequency noise, charge pumping, and other electrical techniques that vary the time scale over which charge exchange between the semiconductor channel and near-interfacial dielectric. Oxygen vacancies and hydrogen impurity complexes are common border traps in a wide variety of systems subjected to bias-temperature stress. Charge trapping and emission tend to dominate observed bias-temperature instabilities for as-processed devices at higher oxide electric fields ($>$ 4–6 MV/cm), and for irradiated devices. Hydrogen diffusion and reactions become relatively more significant in as-processed devices at lower electric fields ($<$ 4–6 MV/cm).

1. Introduction

Interface, oxide, and border traps play key roles in determining the magnitude and time dependence of bias-temperature instabilities in MOS devices and ICs [1–8]. Each type of defect can affect both the short and longer term performance degradation of a device, depending on the density and energy distribution of the defects, as well as the spatial distributions of oxide and border traps. The microscopic origin and impact of bias-temperature instabilities remains a topic of great interest [6–14]; here we discuss the role of border traps, with a focus on the nature of these defects and techniques to estimate their effective energies and effective energy distributions.

The effects of border traps on the performance, reliability, and radiation response of MOS devices can be significant. Their impact on threshold voltage, transconductance, current drive, speed, and other DC and AC operating parameters are determined by both the "heredity" and the environment of the defect. A border trap typically has similar microstructure to oxide (or bulk) traps because it shares the same growth conditions and approximately the same local stoichiometry [2,7,8,15–21]. However, its proximity to a dielectric/semiconductor interface often modifies the defect energy level relative to the band edge, and/or greatly enhances the probability that a channel carrier can tunnel into the near-interfacial dielectric layer [15]. For highly scaled devices, a similar defect that lies within convenient tunneling distance of both a semiconductor (channel) and metal (gate) interface can greatly enhance the gate current via trap-assisted tunneling [22–25]. Here we focus primarily on the properties of devices in which border traps lead to threshold voltage shifts and/or transconductance degradation as a result of charging/discharging during bias-temperature stress.

In this overview we first discuss defect nomenclature, and show examples for the Si/SiO_2 system that show the importance of oxygen vacancies and hydrogen in determining effective border-trap densities for devices subjected to bias-temperature stress and/or ionizing radiation exposure. Additional results are shown for high-K dielectrics on Si, Ge, and InGaAs. Challenges are discussed in separating effects of interface, oxide, and border traps for wide band gap semiconductors. Finally, we briefly discuss border traps in MOS devices with graphene, carbon-nanotube, and black-phosphorus channels.

2. Background

The term "border trap" was introduced as a way to attempt to harmonize and more precisely describe the effects of near-interfacial oxide traps on the performance, reliability, and radiation response of MOS devices and ICs [2,15]. The term derives by particular analogy

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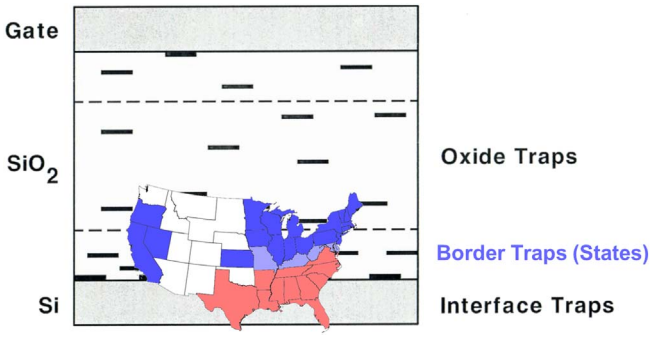

Fig. 1. (Color on line.) Schematic illustration showing oxide, interface, and border traps (states) in MOS devices. Border traps are near-interfacial oxide traps that exchange charge with the underlying semiconductor channel on the time scale of the measurements of interest. This nomenclature was inspired by the analogy with border states in the US Civil War (inset). Border states (lighter blue) were politically a part of the Union (North – darker blue), but owing to their proximity to the Confederacy (South – red), they retained strong cultural and emotional ties to the South.(For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.) (After Fleetwood [15], © IEEE, 1992; inset after Wikipedia [26].)

with the "border states" that played significant roles in the US Civil War, as shown schematically in Fig. 1 [15,26]. This particular association is not unique. Border regions are universally of significance in a number of geographical regions and fields of study; one is as likely in political science or history to discuss the importance of a border region as in science or engineering. Other terms for these defects include slow states (or traps), anomalous positive charge, switching oxide traps, near-interface oxide traps, etc. [2,7,10,15,17,27–31]. Particularly in publications before the early 1990s, the effects of border traps were often lumped together with effects of interface traps, many of these terms were often used interchangeably, and border traps were often mistaken for interface traps. In the last 25 years, discussions have become more focused on distinguishing among these effects, and the effects of border traps have become more significant in highly scaled technologies with high-K dielectrics and alternative channels to Si [9,15,32,33].

Spectroscopic evidence, e.g., from electron paramagnetic resonance (EPR), spin-dependent recombination, etc. is important to distinguishing the effects of interface and border traps [10,16,19,34–37], but because of the relatively low defect densities in technologically relevant materials and the small volumes of the border region in a modern MOS device, direct evidence about defect microstructure is often difficult to obtain. Hence, most works that attempt to identify the effects of border traps rely on electrical measurements, varying in measurement time scale [2,7–14], often supported by first-principles calculations, e.g., via density functional theory [5,7,8,13,38–40].

For narrow-gap semiconductors (e.g., Si, Ge, SiGe), border traps tend to exchange charge more slowly with the underlying semiconductor than interface traps, and true oxide (or bulk) traps tend only to charge under extreme conditions (radiation, high field stress) and discharge over very long time scales (days, weeks, months, years) [2,10,41]. These processes are illustrated schematically in Fig. 2 [41]. The dividing line between interface and border traps depends primarily on the sharpness and distinction of the interface; the line between an oxide trap and border trap depends primarily on the speed of the measurement. Longer measuring times lead to higher effective border-trap densities. For wider band-gap materials (e.g., SiC, GaN), it is often not possible to distinguish between interface, oxide, and border traps using electrical methods alone [10,39,42–51]. A border trap with energy close to the Fermi level can exchange charge with the semiconductor much more readily than a midgap level interface trap under typical device operating conditions. For these devices, as a consequence, unless an extensive series of detailed characterization measurements are performed using a variety of experimental methods, and involving carefully designed processing splits intended to affect interface and border traps differently (challenging to do), the effects of interface and border traps are frequently difficult to separate.

3. Si MOS DEVICES

Low-frequency ($1/f$) noise measurements are often useful in estimating the effective density and energy distribution of border traps in MOS devices [2,8,18,52–55]. The observed noise below ~10 kHz in a SiO_2-based MOS device is due primarily to border traps; noise at higher frequencies can include contributions from interface traps [21,56]. Oxygen vacancies and/or hydrogen-related defect-impurity complexes that often include an O vacancy are the defects that most often function as border traps in MOS devices with SiO_2 gate dielectrics [18–21,27,28]. For example, in a series of studies [52,54–57], a strong correlation was demonstrated between the low-frequency noise of MOS transistors and oxygen vacancies in SiO_2. For example, Fig. 3 shows a direct correlation between the pre-irradiation magnitude of the normalized low-frequency noise K and the post-irradiation threshold-voltage shift due to radiation-induced oxide-trap charge (ΔV_{OT}) [57,58]. It is well known from EPR studies that radiation-induced oxide-trap charge is due primarily to hole trapping at O vacancies in SiO_2 [16,19,59–62]. This strongly suggests that O vacancies in SiO_2 can function as border traps.

Fig. 4 shows the effective border-trap energy distribution for MOS transistors with 32-nm SiO_2 oxides (a) before irradiation, after 500 krad (SiO_2) X-ray irradiation, and (c) after 200 °C post-irradiation annealing at 0 V. The defect-energy distributions for the O vacancy-related defects causing the noise is shown on the upper x-axis, using the Dutta-Horn model of low-frequency noise [63], which has been tested thoroughly and validated for a number of physical systems, including MOS devices, as reviewed in [55]. The effective density of border traps increases with irradiation in Fig. 4 and decreases with post-irradiation annealing. After irradiation and annealing, the shape of the energy distribution is altered significantly, even though the overall defect density has returned close to initial values. This is evidence of defect reconfiguration as a result of the capture and annealing of radiation-induced charge [54].

Additional, strong support for the idea that O vacancies in SiO_2 can function as border traps was provided in spin-dependent recombination studies of irradiated gated diodes, as shown in Fig. 5 [34]. Exposing devices to ionizing radiation leads to hole capture at O vacancies and enhances interface-trap buildup at the Si/SiO_2 interface, enabling spectroscopic identification of the underlying point defects [52,59–62]. The P_b defects are true interface traps, and the E′ defects that are active in these experiments are border traps [15,34].

A schematic model of how an E′ defect near the Si/SiO_2 interface can function as a border trap for an irradiated device is shown in Fig. 6. The positive charge that results from radiation-induced-hole capture remains on one side of the E′ defect, and an electron tunnels between the other side of the defect and the Si in response to changes in gate bias. The dipole formed when the electron is pulled into the SiO_2 under positive bias is a neutral defect, which becomes positively charged when the electron is forced out of the oxide under negative bias [17,64,65]. This model is supported for irradiated MOS devices by EPR studies [19], as well as by a number of irradiation and annealing studies [17,62,65,66]. A significant fraction of the electron traps associated with trapped holes in SiO_2 that function as border traps are often quite stable; even years of elevated-temperature annealing may not remove them [66].

We now consider how O vacancy-related defects can function as border traps and lead to $1/f$ noise and/or bias-temperature instabilities in an unirradiated device. The $1/f$ noise of an nMOS transistor before or after irradiation may result from the thermally assisted capture and emission of an electron by a dimer O vacancy (site A in Fig. 6). Defect functional theory (DFT) calculations show the probability of capturing an electron from the Si increases with increasing separation of the Si1-