Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Empirical derivation of upper and lower bounds of NBTI aging for embedded cores

Yukai Chen*, Enrico Macii, Massimo Poncino

Department of Control and Computer Engineering, Politecnico di Torino, Corso Duca degli Abruzzi, 24, Torino 10129, Italy

ARTICLE INFO

Article history:
Received 11 February 2017
Received in revised form 28 June 2017
Accepted 15 July 2017
Available online xxxx

Keywords:
Reliability
NBTI aging
Embedded processors
Modeling
Simulation
System-level models

ABSTRACT

In deeply scaled CMOS technologies, device aging causes transistor performance parameters to degrade over time. While reliable models to accurately assess these degradations are available for devices and circuits, the extension to these models for estimating the aging of microprocessor cores is not trivial and there is no well accepted model in the literature.

This work proposes a methodology for deriving an NBTI-induced aging model for embedded cores. Since aging can only be determined on a netlist, we use an empirical approach based on characterizing the model using a set of open *synthesizable embedded cores*, which allows us to establish a link between the aging at the transistor level and the aging from the core perspective in terms of maximum frequency degradation.

Using this approach, we were able to (1) prove the independence of the aging on the workloads which run by the cores, and (2) calculate upper and lower bounds for the "aging factor" that can be used for a generic embedded processor.

Results show that our method yields very good accuracy in predicting the frequency degradation of cores due to NBTI aging effect, and can be used with confidence when the netlist of the cores is not available.

1. Introduction

Aging of CMOS devices has been one of the latest undesired side-effects of technology scaling. Among the many different aging phenomena, negative bias temperature instability (NBTI) has emerged as one of the most crucial factors in shortening the lifetime of devices [1]. A large bulk of research has addressed the issue of NBTI-induced aging from the modeling and optimization perspectives; they have been generally focused on logic blocks and SRAM structures because accurate characterization of NBTI aging *requires the availability of the circuit netlist* in order to extract critical paths and the signal probabilities of the relative cells. These information are easily available for logic circuits during the synthesis phase, and are implicit for SRAM structures, whose topology is well-defined.

Extending this analysis to processor cores, however, is a quite different matter. In the typical design scenario, cores are in fact regarded as black-box, third-party IPs whose netlists are obviously not available. As a consequence, the state of the art in the modeling of the aging of a core is limited to very simple approximations based on the power states of the core: the core will age according to some constant *aging factor* when active, and it will not age (or recover) when idle. Aging and recovery are estimated assuming a baseline aging model, which can be either analytical (taken from physics, as in [2–6]) or empirical (derived by fitting data as in [7]). While some differences exist among the various approaches ([2–7]), this state-based aging model is the underlying common paradigm.

One problem with these approaches is that the assumption of a constant "aging factor" is not motivated nor validated. In fact, as [3] states, "*there is no publicly-available validated information on expected service life and aging rates of processors*". Therefore, previous works provide little or no hint on how this factor can be computed, and how a factor applicable to one core can be applied to a different one. Furthermore, the underlying models used in these works refer to the model for a single logic gate; however, in order to fully characterize the aging rate of a core, a more complex model should be used.

The limitations of these works are a consequence of the fact that an accurate characterization of the value dependency of NBTI is *only possible through an accurate logic simulation of the netlist*. The true NBTI aging of the critical path depends on the signal probabilities of the gates it contains; without these information only coarse approximations are feasible.

In this work, we determine such aging factor by using an empirical analysis on a set of open, synthesizable cores for which a gate-level netlist can be obtained. We target embedded processor cores with typical RISC architectures, for which we can have a better degree of confidence about the generality of the presented results.

* Corresponding author at: Politecnico di Torino, Department of Control and Computer Engineering, Corso Duca degli Abruzzi, 24, Turin 10129, Italy.
E-mail addresses: yukai.chen@polito.it (Y. Chen), enrico.macii@polito.it (E. Macii), massimo.poncino@polito.it (M. Poncino).

http://dx.doi.org/10.1016/j.microrel.2017.07.067
0026-2714/

Our ultimate objective is in fact to derive an aging factor that is as much general as possible and applicable to a generic core, in particular when its netlist is not available.

The core netlists are used to obtain detailed aging data by running a set of application kernels as data for characterization and using a logic simulator augmented with transistor aging models [8]; aging data are then used to fit an underlying aging macromodel. Statistical correctness of the evaluation is guaranteed by using different datasets for the characterization and different cores for the validation.

The following are the main results that we obtained from our analysis:

1. We show that aging of the core is independent of the workload. Quite surprisingly, the impact of different applications and different datasets have negligible impact on the aging of the embedded core. As further elaborated in the paper, this is mainly due to the characteristics of the critical paths that determine the maximum frequency of the core; in practice, different executed instructions and data do not alter significantly the probability values on the critical paths.
2. A direct consequence of the workload independence is that, for a given core, it is possible to define a fixed aging factor, to be interpreted as an equivalent signal probability to be used in a traditional transistor-level aging model. This is the most relevant result of our work.
3. Since in general any core will have its own aging factor because of differences in the architecture or different synthesis constraints, deriving a single, "universal" aging factor good for any embedded core is generally not feasible. However, the characterization on different architectures and with different synthesis constraints allows to yield lower and upper bounds for the aging factor. They can be used with a high degree of confidence for any embedded core having comparable complexity to those used in our characterization. Notice that these bounds are not related to different workloads but just to different architectures and different synthesis constraints.
4. Based on these outcomes, we propose a practical NBTI aging macromodel for a core that is a generalization of the traditional transistor-level one, where aging is expressed as a degradation of the maximum working frequency F_{max} and the best- and worst-case aging scenarios can be inferred based on the aging factor range.

Our validation is simulation-based, and is done on one of the synthesizable cores that was not used for the characterization. In this way we were able to compare the actual aging on the netlist with the bounds provided by the aging factor range applied to the macromodel. The comparison shows extremely good accuracy, with a maximum error of 2.88%.

The manuscript is organized as follows: in Section 2 we describe the background on NBTI and works related to our contribution. Section 3 presents the methodology used for characterization and to derive the proposed NBTI aging model; the reference embedded cores platforms are illustrated in Section 4. In Section 5 we present the results of the model characterization phase, while Section 6 shows our derived model and its relative validation by comparison of estimated and simulated results. Finally, Section 7 discusses a few perspectives and possible enhancements to the proposed model.

2. Background and previous work

2.1. Background

Among the many different device aging mechanisms, NBTI is regarded as the most critical one. It causes a gradual increase in threshold voltage (V_t) and occurs when a pMOS transistor is negatively biased, that is, when $V_{gs} = -V_{dd}$, corresponding to a logic "0" being applied to the gate of a pMOS transistor (the *stress* state); the increase of V_t absolute value causes then a degradation of the delay of the device. Conversely, when a logic "1" is applied to the pMOS gate, NBTI stress is partially removed (the *recovery* state), resulting in a decrease V_t absolute value.

A compact and general model of NBTI-induced V_t drift for a transistor can be written as follows:

$$\Delta V_t = \alpha \cdot f(V_{dd}, V_t, T, \mathbf{R}) \cdot g(t). \quad (1)$$

The model has three main factors:

1. A term α denotes the *aging factor* which depends on (i) the actual stress/recovery pattern (i.e., time spent with the two logic values at the inputs) and is also affected by the activity (i.e., the time spent in active model) of the device.
2. A term including all technological and environmental parameters ($f()$): the degradation by NBTI depends on operational parameters, supply voltage V_{dd}, threshold voltage V_t, temperature T, and all the device parameters, lumped here for compactness into set $\mathbf{R}$, comprising for instance oxide geometrical and electrical parameters, activation energy, device size, and load. For the precise mathematical expression of $f()$ the reader is referred to classical NBTI overview paper [1].
3. A function $g(t)$ modeling the dependence over time of the drift. The shape of the function depends on the physical mechanism adopted to explain the NBTI effect [9]. Examples are the reaction-diffusion (R-D) model, for which $g(t) = t^n$, [9] indicates the values of n in the R-D model. Or the hole trapping (HT) one, for which $g(t) = 1 - e^{t^n}$, [10] shows that the reported time exponent n from previous works has a wide spread from 0.1 to 0.3; it also observes that n is around 0.2 can yield 90% accuracy NBTI aging under real use conditions. The work of [11] presents a thorough comparative analysis of the two models at the gate-level, and shows both models match well to obtain the NBTI degradation signature as a function of the *gate type*, *drive strength*, *input frequency*, and *the duty factor*. While in terms of *non-periodicity*, *instant degradation vs. long term degradation*, *CPU time* and *memory usage*, the two models show the different performance on these aspects. For example, the Atomistic trap based model can target the degradation simulation as fast as *ns* stress time, but cannot target the longer stress simulation; on the other hand, R-D model simplifies the BTI interpretation as a slow mechanism in order to speed-up the long-term stress simulation. The authors of [12] also give a review of R-D model and charge trapping model. Moreover, we refer the reader to [13] for the latest charge-trapping NBTI model. In this work we adopt the R-D model for our analysis since the technology library we used already includes the V_t drift information for a R-D model, and specifically $g(t) = t^{1/4}$ based on the technology library provided by *STMicroelectronics*.

For a given combination of environmental conditions, technological values, and $g(t)$, it is the value of α determines the actual V_t drift. Thanks to some mathematical properties of NBTI aging mentioned in [15], it can be shown that it is possible to use *signal probabilities* instead of actual signal values for the evaluation of the effective stress. It is worth remarking that the model of Eq. (1) technically applies to an individual transistor and, with minor adaptation, to a logic gate. The translation of the V_t drift on a more macroscopic

Please cite this article as: Y. Chen et al., Empirical derivation of upper and lower bounds of NBTI aging for embedded cores, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.07.067