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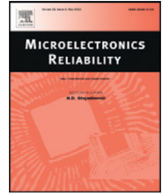

Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement

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ABSTRACT

Transient thermal impedance measurement is commonly used to characterize the dynamic behaviour of the heat flow path in power semiconductor packages. This can be used to derive a "structure function" which is a graphical representation of the internal structure of the thermal stack. Changes in the structure function can thus be used as a non-destructive testing tool for detecting and locating defects in the thermal path. This paper evaluates the use of the structure function for testing the integrity of the thermal path in high power multi-chip modules. A 1.2 kV/200 A IGBT module is subjected to power cycling with a constant current. The structure function is used to estimate the level of disruption at the interface between the substrate and the baseplate/case. Comparison with estimations of cracked area obtained by scanning acoustic microscopy (SAM) imaging shows excellent agreement, demonstrating that the structure function can be used as a quantitative tool for estimating the level of degradation. Metallurgical cross-sectioning confirms that the degradation is due to fatigue cracking of the substrate mount-down solder.

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1. Introduction

Degradation of the thermal conduction path is among the dominant failure mechanisms of power semiconductor packages. Typically, solder fatigue results from the thermo-mechanical stresses at the interfacing contacts due to mismatched coefficient of thermal expansions (CTEs) between different materials which constitute the heat flow path causing cracking. The correlation between solder fatigue and the degradation in the thermal performance of power semiconductor packages has been previously reported in the literature [1–4]. Increase in thermal resistance occurs because heat dissipation through the package is compromised by the disruption in interconnection resulting from solder fatigue. There have been some attempts to quantify the correlation between the increment in thermal resistance and the cracked area of solder layers [5–8]. However, all of these studies focused on single chip packages (e.g. TO-247), none of which considered high power multi-chip semiconductor packages. In addition, most of these studies relied on finite-element modelling (FEM) to quantify the relationship between unattached area and thermal resistance.

Thermal transient measurement is a common characterization method of the heat conduction path of power semiconductor packages. Many researchers have reported that the thermal impedance of a thermal stack is representative of the internal structure of the thermal stack [9,10]. This fact legitimizes the use of thermal impedance as a non-destructive evaluation tool to detect structural defects in the heat conduction path. Szekely [11] proposed an accurate systematic procedure which allows a mapping of the internal structure based on the thermal impedance measurement. The proposed procedure produces a "structure function" which is a graphical tool that represents the internal structure of the thermal stack of an encapsulated semiconductor package. The structure function can therefore be used as a failure analysis tool to detect, locate and estimate cracking and voiding which results from solder fatigue in power semiconductor packages [11]. This method has been recognized by the "JEDEC" standards series "JESD51" for thermal characterization of packaged semiconductor devices [12].

In this work, the validity of the structure function as a non-destructive evaluation tool for high power multi-chip semiconductor packages is investigated. Junction-to-case thermal resistance R_{thjc} and cracked area, estimated by structure function, are compared to the cracked and unattached area estimated by Scanning Acoustic Microscopy (SAM). For this purpose, a conventional 1.2 kV/200 A IGBT power module is actively power-cycled to degrade the solder at the substrate-base plate interface. SAM imaging is performed at regular intervals at multiple stages of the power cycling test to observe the gradual degradation of the

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solder layer. Thermal impedance measurements are also recorded regularly during the power cycling test and the structure function is calculated. The junction-to-case thermal resistance R_{thjc} and detached area estimated by the structure function are then compared to the cracked area estimated from the SAM images.

2. Theoretical background

To facilitate the interpretation and discussion of the results, it is helpful to briefly review the theoretical background regarding the structure function. It is common for the heat flow path to be represented by an equivalent electrical RC Cauer network. This Cauer-type model is considered to be a physical description of the heat flow path [13]. The structure function is a graphical representation of the components of the Cauer network which represents the heat flow path [11]. The most common methods of Cauer network parameterization rely on material and geometrical properties [14] or on experimental measurement [13] and typically produce models up to the 6th order. However, in order to get an accurate representation of the physical structure by the structure function, a higher order Cauer network is required.

Fig. 1. Mentor Graphics Power Tester 1500A used for power cycling test.

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