ARTICLE IN PRESS

Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: <www.elsevier.com/locate/mr>

Validation of TSV thermo-mechanical simulation by stress measurement

Wei Feng ⁎, Naoya Watanabe, Haruo Shimamoto, Masahiro Aoyagi, Katsuya Kikuchi

Nanoelectronics Research Institute (NeRI), National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba Central 1, 1-1-1 Umezono, Tsukuba, Ibaraki, 305-8560, Japan

article info abstract

Article history: Received 17 August 2015 Received in revised form 14 January 2016 Accepted 15 January 2016 Available online xxxx

Keywords: Through silicon via (TSV) Thermal stress measurement Raman spectroscopy FEM simulation

Because of the large mismatch in coefficients of thermal expansion (CTE) between copper vias and the silicon substrate in through-silicon vias (TSVs), thermal stresses are induced. These stresses cause severe reliability issues, such as performance degradation of stress-sensitive devices, and interfacial delamination between TSVs and the silicon substrate. Finite element method (FEM) simulation is a useful tool for thermal stress analysis; however, developers and users are concerned about the range of accuracy of simulation models. Direct validation of the thermal simulation via stress measurement is extremely difficult. As non-destructive methods can measure the stresses only at the surface or several micrometers below, it is difficult to measure the internal stresses. Furthermore, any attempt to use an internal measurement location in the sample affects the stress situation. We propose a methodology to validate the simulation model with stress measurements using polarized Raman spectroscopy on cross-sections of TSV samples. The stress-free assumption at room temperature for simulation was compensated for using the measured residual stresses. An accurate comparison of stress data between experiment and simulation was achieved by considering the re-location of measurement points under thermal deformation. The agreement between simulation and experimental data for radial and axial thermal stresses validated the simulation model.

The validated simulation model is useful for structural parametric analysis of TSV. The proposed methodology with stress measurement by polarized Raman spectroscopy and stress analysis by simulation can be used to study the radial and axial thermal stress of other devices.

© 2016 Elsevier Ltd. All rights reserved.

1. Introduction

Three-dimensional (3D) technologies provide volumetric packaging solutions to achieve higher integration, higher-speed signal transmission, reduced power consumption, and smaller footprints [\[1\]](#page--1-0). Through silicon vias (TSVs), used to fabricate 3D vertically stacked devices, including logic, memory, sensors, and actuators, play a key role as interconnects in 3D miniaturization of electronic devices [\[2,3\]](#page--1-0).

The large mismatch in coefficients of thermal expansion (CTE) between copper (Cu) vias and the silicon (Si) substrate in TSVs induces thermal stresses, which lead to electrical performance degradation and various reliability issues, such as device characteristic deviation due to stress in Si substrate. S. Thompson et al., reported that 100 MPa of stress can change carrier mobility by more than 7% in MOSFET devices [\[4\]](#page--1-0). Therefore, research into thermal stress levels in Si substrates is important for minimizing device characteristic deviation.

FEM simulation is increasingly being used for studying 3D technologies [\[5](#page--1-0)–7]. However, it is important to note that FEM is applied to an

Corresponding author. E-mail address: wei.feng@aist.go.jp (W. Feng).

<http://dx.doi.org/10.1016/j.microrel.2016.01.007> 0026-2714/© 2016 Elsevier Ltd. All rights reserved. approximate mathematical model of a system because of the complexities in the geometry, properties, and boundary conditions of most realworld problems. The developers and users of simulation models are concerned with whether models and their results are accurate.

A large amount of research into the thermal–mechanical characterization of TSVs has been carried out using FEM simulations [8–[11\].](#page--1-0) Commercially available FET software such as ANSYS and ABAQUS was widely used for via-level, chip-level, and wafer-level stress simulation of 3D technologies [12–[14\].](#page--1-0) However, among these studies, there are few reports that include validation of the simulation results with stress measurements.

Thermal stresses can be evaluated using Raman spectroscopy, X-ray diffraction (XRD), digital image analysis (DIA), or Piezo stress sensor TEG (test element group) to validate the simulation model [15–[18\].](#page--1-0) Among these methods, Raman spectroscopy has been widely used to nondestructively investigate stresses [\[19,20\].](#page--1-0) It has been reported that stress results via simulations matched the trend of μ-Raman spectroscopy measurements [\[21\]](#page--1-0). M. A. Rabie et al. reported that the difference between the stress in simulations and measurements could be attributed to residual stresses [\[22\]](#page--1-0). Non-destructive methods can only measure the stresses at the surface or several micrometers below. However, any destructive action, such as cutting to obtain a cross-section, or

Please cite this article as: W. Feng, et al., Validation of TSV thermo-mechanical simulation by stress measurement, Microelectronics Reliability (2016), <http://dx.doi.org/10.1016/j.microrel.2016.01.007>

2 W. Feng et al. / Microelectronics Reliability xxx (2016) xxx–xxx

Fig. 1. Fabrication process for copper-filled TSV samples for thermal stress measurement.

chemical mechanical polishing (CMP), changes the stress situation; thereafter, the measured stresses no longer indicate the original stress level. To the best of our knowledge, agreement between simulation and measurement of internal thermal stress has not yet been reported.

In this study, we performed both stress measurement and FEM simulation analysis on a cross-section of a Cu-filled TSV. To determine the temperature dependence of the TSV thermal stresses, radial and axial stress measurement was performed at three points on the Si substrate of the TSV cross-section using polarized Raman spectroscopy under three temperature conditions. The influence of the thermal deformation on the three measuring points was considered during the extraction of simulation results. Furthermore, the stress-free assumption at room temperature in the simulation was compensated for by measuring the residual stresses as offsets. We compared both radial and axial thermal stresses in simulations to measurement data to validate the simulation model.

2. TSV sample preparation and stress measurement using polarized Raman spectroscopy

The thermo-mechanical stress measurement of a cylindrical regular Cu-filled TSV was performed in this study. The TSV sample size is 10 μm in diameter and 58.5 μm in depth. The TSV sample was fabricated using a via-last approach (Fig. 1) as follows:

- \geq RIE (reactive ion etching) on a Si wafer
- \geq Oxide film deposition using sub-atmospheric chemical vapor deposition (SACVD)
- \geq Tantalum and Cu films applied by sputtering
- \blacktriangleright Cu Electroplating
- ➢ CMP
- \triangleright RDL (re-distribution layer) formation
- ➢ Photoresist and Cu seed removal

Fig. 2. Optical microscope images of the cross-section of the Cu-filled TSV sample. Stress measurements were performed at three points on the Si substrate at 0.5 μm from the top of the $Si/SiO₂$ interface and $1/3/5$ µm from the TSV edge using polarized Raman spectroscopy.

Fig. 3. Measurement configuration of polarized Raman spectroscopy. An exciting laser light was placed on the surface of the TSV's cross-section. Then, the scattered light was detected by the spectrometer.

Then, the annealing process was performed for the TSV sample.

The TSV was subjected to CMP to reveal its cross-sectional surface for internal stress measurement. Then, the local stress in a Si substrate along the vertical (z) axis, and the stress under the boundary condition with the top insulator layer can be analyzed. An optical microscope image of the TSV is shown in Fig. 2.

The stress measurement was performed on the TSV cross-sections using polarized Raman spectroscopy (Ramanor U-1000) at TORAY Research Center using the measurement configuration shown in Fig. 3 [\[23\].](#page--1-0) An un-doped bare Si wafer was used as a stress-free reference. An exciting light at the 457.9-nm line of an argon ion laser was used for the Raman measurements. Fig. 4 shows the polarization vector of exciting and scattered light for polarized Raman spectroscopy. The exciting lights were directed at the measuring cross-section of the [110] surface. Then, the scattered lights from the cross-section surface of the TSV sample were dispersed using a Jobin Yvon U1000 double monochromator; then detected for the [110] directions, as directions [001] for axial stress and [110] for radial stress. The spatial resolution of the polarized Raman spectroscopy is 0.7 μm, which is the laser spot diameter. The probing depth in the current measurement setup is 140 nm. Assuming uniaxial or non-isotropic biaxial stress σ_{11} along the [100] direction and σ_{22} along the [010] direction on a (001) face of silicon, the Raman frequency shift Δω can be expressed using elastic compliance S and phonon deformation potentials p and q as follows [\[23\]](#page--1-0):

 $\Delta \omega_3 = [pS_{12} + q(S_{11} + S_{12})](\sigma_{11} + \sigma_{22})/(2\omega_0)$

The frequency shift of optical phonons is proportional to the combined stress $\sigma_{11} + \sigma_{22}$. The plasma lines from the argon ion laser were

Fig. 4. Measurement technique: polarization vector of exciting and scattered light of polarized Raman spectroscopy. The scattered light from the cross-section surface of the TSV sample was dispersed, then detected in the [110] direction.

Please cite this article as: W. Feng, et al., Validation of TSV thermo-mechanical simulation by stress measurement, Microelectronics Reliability (2016), <http://dx.doi.org/10.1016/j.microrel.2016.01.007>

Download English Version:

<https://daneshyari.com/en/article/6946282>

Download Persian Version:

<https://daneshyari.com/article/6946282>

[Daneshyari.com](https://daneshyari.com)