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Design considerations for the mechanical integrity of airgaps in nano-interconnects under chip–package interaction; a numerical investigation

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ABSTRACT

Airgaps can undermine the mechanical properties of nano-interconnects and lead to reliability issues such as back end of line (BEOL) fractures. In this context, interconnect delamination under chip–package interaction (CPI) induced loads is a major failure mode which benefits from in-depth investigation. In this computational study, models of airgaps fabricated using the etch-back approach are developed for 90 nm pitch interconnects and potential mechanical failure modes including the fracture energy release rate (ERR) at various material interfaces are investigated. In addition, capacitance benefits of airgap implementation compared to the mainstream low-k technology are calculated using a capacitance simulator. Subsequently, mechanically conscious airgap design strategies are proposed which allow taking advantage of the maximal capacitive benefits of airgaps and limit the CPI related reliability concerns.

1. Introduction

Interconnect resistive and capacitive delay is a major limitation for the performance of ultra large scale integration (ULSI) integrated circuits [1]. Specifically, interconnect capacitance, increases cross-talk and power dissipation which has motivated the development of novel inter-line ultra-low-k dielectric materials (ULK) with k values lower than 2.5 [2]. In spite of that, reduction of k value usually entails inferior mechanical properties such as lower stiffness, low fracture toughness and inferior adhesion of ULK materials which undermines the mechanical integrity of back-end of line (BEOL) under chip–package interaction (CPI) loads [3,4]. This mechanical deterioration mainly occurs due to inclusion of pores to the structure of ULK materials and also implementation of materials with weaker chemical bonds for reducing the k value [3–5]. Such inferior mechanical characteristics constitute a limit for further reduction of the effective k value because of reliability concerns. In this context, another approach which has attracted significant attention and effort in the microelectronics sector is the integration of airgaps at the interline space [6–11] as an alternative for the low-k materials given that air offers the best dielectric constant value of 1. However, implementing airgaps potentially constitutes a BEOL reliability concern specifically from a CPI performance standpoint [12,13].

Recently, the etch-back approach where the inter-line dielectric is removed by an etch step has been shown to be a promising airgap integration method [11,14]. In this approach, in order to ensure mechanical and chemical stability, a relatively stiff and hermetic dielectric liner is conformally deposited to cover the metal and gap structure which prevents oxidations and also provides mechanical support and stability to the airgap and metal lines [11,14]. Albeit, as the inter-line space is down-scaled it is necessary to reduce the thickness of the liner or use materials with lower k value in order to maximize capacitance reduction which potentially compromises the mechanical strength of BEOL under CPI loads. The study of the mechanical impacts of the design of airgaps fabricated using the etch-back approach, is scant in the literature. Therefore, in this computational study finite element (FE) models of interconnect structures are developed in order to investigate the mechanical implications of airgap inclusion in BEOL using this approach. Specifically, airgap design strategies to minimize delamination and maximize airgap capacitance benefits are investigated.

2. Methods

2.1. CPI and delamination simulations

2.1.1. Model geometry

A 3D FE model of a four level interconnect structure was developed within the MSC.MARC® FEM package (http://www.mscsoftware.com/product/marc). The model has a square cross section and includes three lines at metal one and metal two levels which have a 90 nm pitch and a 45 nm CD, see Fig. 1. Dummy metal three and four layers were included with mechanical properties of copper to realistically recapitulate the

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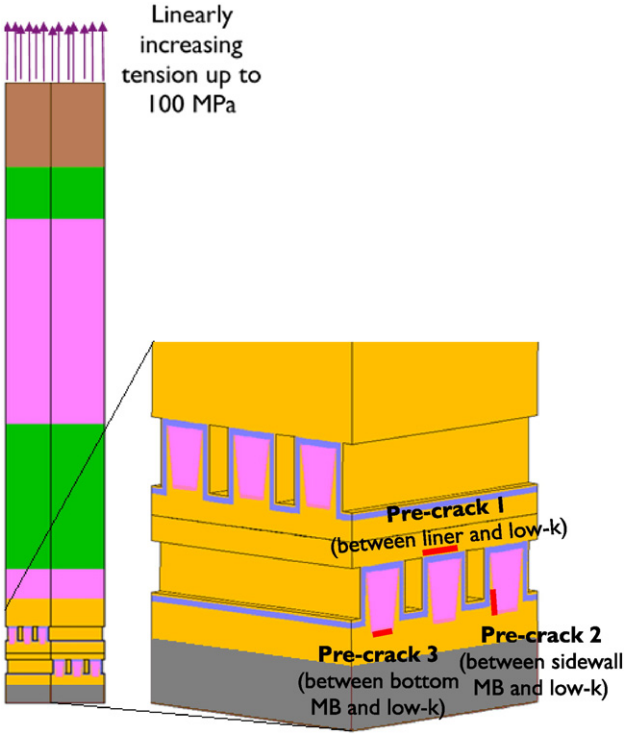

Fig. 1. The 3D model of the 4 layer interconnect developed for the simulations. Yellow showing the ultra low-k (ULK) material, blue the dielectric liner, light pink depicting copper lines, dark pink showing the metal barrier, green showing the silicon dioxide dielectric, gray layer at the bottom of the stack showing a dummy layer representing the intermetallic layer and the brown layer on the top of the BEOL stack depicting the silicon nitride passivation. The red lines represents the pre-cracks implemented in the model.

mechanics of a BEOL stack. Silicon dioxide was incorporated as the dielectric in metal three and four levels and either ULK or airgaps were incorporated in metal one and metal two levels. The model was constructed by creating the 3D mesh within MSC.MARC. The model approximately consisted of 22,000 full integration, linear hexahedral solid elements (type 7 in MSC.Marc). The Layer 1 of the BEOL stack was attached to the Layer 2 using the glue contact behavior and the surface to surface contact discretization was used. Also, the thickness of the dielectric liner was varied from 2 nm to 10 nm in a parametric study. The lower range of the dielectric liner thickness (i.e. 2 nm) was chosen given the technological limitations which render deposition of thinner dielectric liners troublesome. In addition, very thin dielectric liners do not provide hermetic properties. The highest dielectric liner thickness was limited to 10 nm due to the capacitive implications given that for the analyzed dielectric liner materials thicknesses above 10 nm will not offer any capacitive benefit. Another aspect in airgap design which can impact the mechanical reliability of interconnects is the influence of airgap depth and height which were also investigated using a parametric study.

In order to understand the influence of the aforementioned parameters on potential delamination, the virtual crack closure technique (VCCT) was employed [15] whereby a pre-crack was implemented at potential delamination interfaces i.e. (i) pre-crack 1 at the top of the metal lines between the via level low-k dielectric and the dielectric liner (ii) pre-crack 2 at the sidewall between the MB and the dielectric and (iii) pre-crack 3 at the bottom of the line between the MB and the low-k dielectric as shown in Fig. 1. The pre-cracks where considered to be rectangular. The pre-crack inclusion locations are motivated by the critical energy release rate measurements which show that essentially the interfaces involving the ULK suffer from the lowest adhesion and that experimental CPI induced Interconnect failure analyses show that cracks initiate from and propagate along these interfaces [4,16–18]. These cracks are mainly driven under tensile mode I opening which constitutes the most critical failure mode of ULK materials [19]. The width of the pre-cracks at the top of the line was equal to half of the line width in all simulations plus the thickness of the dielectric liner. At the bottom of the line the width of the pre-crack was assumed to extend the entire width of the line. At the sidewall the pre-crack has a width equal to half of the line side length. The length of all pre-cracks is considered to extend to the total length of the metal line in the RVE which is 270 nm.

2.1.2. Mechanical material properties

Materials in advanced nano-interconnects, are widely considered to behave in a linear elastic manner and the failure mode is based on brittle fracture and delamination. This is mainly due to the low fracture toughness and adhesion of the low-k dielectrics and the dramatic dimensional down-scaling of copper lines. We have previously shown these brittle fracture events in dedicated experimental studies which also showed that linear elastic material properties can address mechanics of materials in nano-interconnect [4,16–19]. The Young's modulus of the low-k dielectric was varied from 3.5 GPa to 8 GPa in a parametric study to investigate the influence of dielectric stiffness on potential delamination. This range is chosen based on the stiffness values for low-k dielectrics used in advanced nano-interconnect [17]. In addition, the stiffness of the dielectric liner was varied between 100 GPa to 350 GPa which covers the Young's moduli of dielectric liner material candidates such as carbon-doped silicon nitride, silicon nitride and aluminum nitride [12,20]. Table 1, summarizes the material mechanical properties used in the parametric studies.

2.1.3. Mechanical boundary conditions

The bottom surface of the BEOL model was fully constrained in the vertical direction and the four lateral surfaces of the representative volume element (RVE) were constrained in the orthogonal directions to the surfaces. A tensile stress increasing in value from 0 to 100 MPa (as a typical stress value that BEOL endures) was applied to the top surface of the RVE to recapitulate the influence of BEOL stresses under CPI loads given that the tensile loading configuration is the most critical mode for BEOL stack failure. The analyses presented are focused on the trends in the ERR variations based on design parameters and as such the absolute value of the max stress applied does not impact the analyses presented. Crack propagation was not allowed in the simulations and only energy release rates for the aforementioned pre-cracks were investigated assuming non-propagating pre-cracks.

In the meanwhile, the impact of each of the aforementioned design parameters on interline capacitance was investigated to ensure that in addition to mechanical optimization, maximum capacitive benefits are achieved. The thickness of the metal barrier (MB) was kept constant at 3 nm in all simulations and copper line dimensions were also kept constant across all simulations.

2.2. Capacitance analysis

Capacitance models of the interconnect structure were developed using the Raphael™ field solver [14,21] and the various designs were simulated consistent with the case studies discussed for the mechanical model by interfacing the Raphael™ with the Optimus™ software. The capacitance of the airgapped interconnects with a pitch of 90 nm and CD of 45 nm and line aspect ratio of 2 were benchmarked against a

Table 1
Mechanical properties used in the simulations [12,20].

Material	Young's modulus (GPa)	Poisson's ratio
ULK 2.4 (organo-silicate glass)	9	0.2
Copper	117	0.3
Carbon doped silicon nitride (SiCN)	100	0.24
Silicon nitride (SiN)	265	0.27
Aluminum nitride (AlN)	350	0.24
Metal barrier (Tantalum MB)	186	0.34