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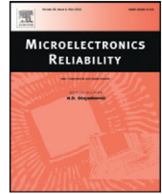

Evaluation of hybrid bonding technology of single-micron pitch with planar structure for 3D interconnection

Masaki Ohyama [a,1], Masatsugu Nimura [a,1], Jun Mizuno [a,*], Shuichi Shoji [a], Toshihisa Nonaka [b], Yoichi Shinba [b], Akitsu Shigetou [c]

[a] Waseda University, 3-4-1 Okubo, Shinjuku, Tokyo 169-8555, Japan
[b] Toray Industries Inc., Electronic & imaging Materials Res. Labs., 3-1-2 Sonoyama, Otsu, Shiga 520-0842, Japan
[c] National Institute for Material Science, 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan

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ABSTRACT

In this paper, we describe hybrid bonding technology of single-micron pitch with planar structure for three-dimensional (3D) interconnection. Conventionally, underfill method utilizing capillary force was used after the bonding of microbump. However, the filling becomes insufficient in a gap less than 10 μm between chips or bumps. One promising technology is the hybrid bonding technology that microbumps and an adhesive can be simultaneously bonded. To realize a single-micron pitch hybrid bonding, we fabricated a planar structure that consists of 8 μm-pitch Cu/Sn microbumps and a non-conductive film (NCF) by a chemical mechanical polishing (CMP) of resin. After planarization, the Cu/Sn bumps and the NCF were simultaneously bonded at 250 °C for 60 s. Cross-sectional scanning electron microscope (SEM) images and energy dispersive X-ray spectroscopy (EDX) images show that the adhesive resin on the bump surface was successfully removed by the CMP. In addition, SEM images of the bonded sample show that the adhesive filled the 2.5-μm gap between the chip and substrate. The Cu/Sn bumps were properly bonded in a corner on the chip. The proposed bonding method is expected to enable single-micron pitch interconnection for ultra-high density 3D LSI of next generation.

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1. Introduction

Three-dimensional large-scale integrated circuit (3D LSI) is a promising technology that is employed to improve the performance of two-dimensional (2D) LSI. 3D LSI has a number of advantages such as reduced packaging area, reduced interconnect delay time, and low power consumption. In 3D integration, LSI chips are vertically stacked with through silicon vias (TSVs) and microbumps [1–4]. Because of an additional requirement for high performance and high density, 3D LSI requires a greater number of next-generation fine-pitch interconnections with microbumps that are less than 10 μm in size [5,6]. Therefore, a new underfilling technology is also needed to fill the ultra-narrow gaps that exist between stacked chips with such fine-pitch microbumps. Underfill is a key technology for a flip-chip bonding because it prevents occurrence of short circuits between microbumps, and protects the microbumps from corrosion and mechanical stress [7,8].

Conventionally, underfill is injected into gaps between stacked chips using capillary force, i.e., the so-called capillary underfill (as shown in Fig. 1 (a)) [9]. However, in the capillary underfill, it becomes difficult to inject underfill resin into narrow gaps between chips without voids that are less than 10 μm because of flux residues and surface tension morphology [10].

Alternate processes of capillary underfill include no-flow underfill and wafer-level underfill (as shown in Fig. 1 (b)) [11–14]. These underfill materials are applied on the chip before a bump bonding. Therefore, the bump interconnection and underfilling are simultaneously achieved. This enables fine-pitch micro-joints to be easily filled without conventional underfill flowing using a capillary force. However, the underfill material can be trapped in the interface between the bonded microbump and the pad [13]. The trapped underfill materials at a bonding interface increase resistance of the interconnection and reduce connection reliability.

One promising solution to address these challenges can be the hybrid bonding process (as shown in Fig. 1 (c)) [15–19]. In this process, excessive underfill material that is over-coated on the microbumps of the chip is removed before a bonding. With this bonding structure, microbumps can be correctly bonded without trapping of the underfill material. Furthermore, narrower gaps between the bonded chips that are less than 10 μm in size are also simultaneously filled. As one of the methods to remove the underfill material, a mechanical surface planarization technique using a diamond bit cutting was reported [15]. Since both the metal and the adhesive were mechanically cut, the cut surface can be easily scratched.

* Corresponding author.
E-mail address: mizuno@waseda.jp (J. Mizuno).
[1] Double first author.

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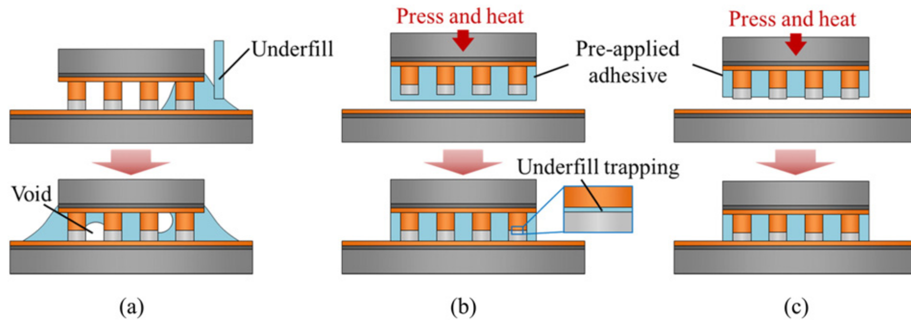

Fig. 1. Schematic illustrations of underfilling processes. (a) Capillary underfill. (b) Wafer-level underfill. (c) Hybrid bonding.

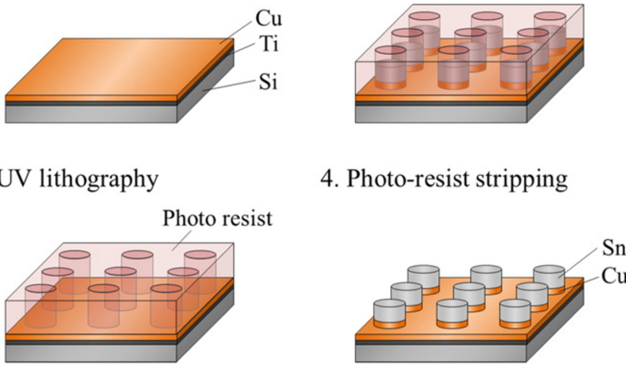

Fig. 2. Process of test vehicle fabrication.

In our previous work, we developed a fabrication method of the planar structure using a chemical mechanical polishing (CMP) of a resin for the hybrid bonding [17]. An uncured adhesive applied on a Si chip with microbumps was removed using the CMP. While some fabrication methods of bonding structure composed of exposed microbumps and an adhesive was proposed, it is not reported to apply the methods to microbumps with pitch of less than 10 μm. In this study, we evaluated the hybrid bonding of single-micron pitch with the planar structure fabricated using the CMP for ultra-high density 3D LSI [20].

2. Experiment

2.1. Fabrication of test vehicle

To evaluate the hybrid bonding, we prepared a Si chip with Cu/Sn bumps and a Si substrate with a Ti/Cu/Au film. Both the chip and the substrate were fabricated based on Si with a thickness of 525 μm.

A fabrication process of the test chip is shown in Fig. 2. First, seed layers of Ti and Cu were sequentially deposited on the chip by electron beam (EB) evaporation. The thickness of each layer was 30 nm and 500 nm, respectively. Second, a 5 μm-thick photo resist was spin-coated on the Ti/Cu layer and formed into hole-patterns with a single-micron pitch using photolithography. Third, a 1 μm-thick Cu and 3 μm-thick Sn were sequentially electroplated on the Ti/Cu layer to fill the patterned holes. Conditions of the electroplating are shown in Table 1. The bump diameter and bump pitch were 4 μm and 8 μm, respectively. Finally, the photo resist was stripped using organic solvent. On the other hand, the Ti/Cu/Au film on the test substrate was also deposited by EB evaporation. The thickness of each layer was 30, 500, and 30 nm respectively. This bonding process relied on interdiffusion between Cu with a high melting point and Sn with a low melting point when the temperature exceeds the Sn melting point (231.9 °C). Hence, Cu oxidization impedes the diffusion of solid-phase Cu into liquid-phase Sn. The Au layer was therefore deposited on the Ti/Cu layer to protect the Cu from oxidization. The design specifications of the test vehicle are summarized in Table 2.

2.2. NCF lamination and planarization by CMP

In this experiment, non-conductive film (NCF, Toray Industries Inc.) was used as the pre-applied adhesive material. Fig. 3 shows a process of

Table 1
Cu/Sn electroplating conditions.

	Cu	Sn
Electroplating bath	Cu sulfate bath	Sn sulfate bath
Current density	2 mA/cm^2	3 mA/cm^2
Time	20 min	20 min
Temperature	25 °C	25 °C

Table 2
Design specifications of test vehicle.

	Chip	Substrate
Size	6 mm × 6 mm	10 mm × 10 mm
Layer thickness	Ti/Cu (30 nm/500 nm)	Ti/Cu/Au (30 nm/500 nm/30 nm)
Bump diameter	4 μm	–
Bump pitch	8 μm	–
Bump height	Cu/Sn (3 μm/1 μm)	–

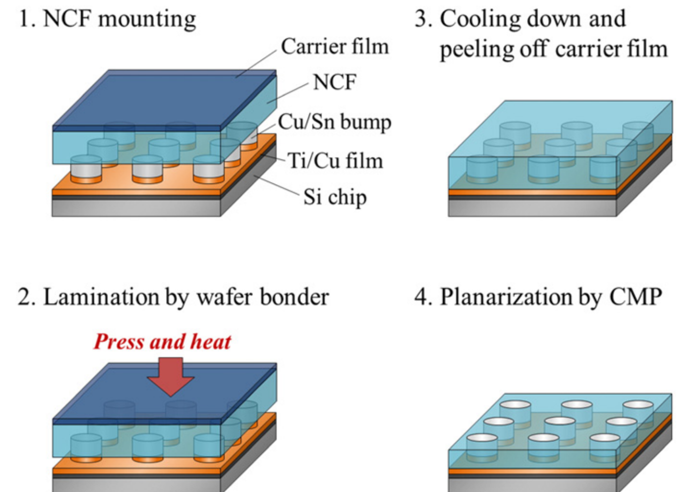

Fig. 3. Process of NCF-laminating and planarization by CMP.

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