Microelectronics Reliability xxx (2015) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

A methodology for projecting SiO_2 thick gate oxide reliability on trench power MOSFETs and its application on MOSFETs V_{GS} rating

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ARTICLE INFO

Article history:
Received 18 May 2015
Received in revised form 17 November 2015
Accepted 30 November 2015
Available online xxxx

Keywords:
Trench MOSFETs
Thick gate oxide
Reliability
TDDB
E-model
Weibull
V_{GS} rating

ABSTRACT

In this work, a methodology based on the E-model for the reliability projection of a thick (>20 nm) SiO_2 gate oxide on a vertical trench power MOSFET, is presented. Experimental results suggest that a Logic Level (LL) trench MOSFET with 35 nm of gate oxide can be rated at $V_{GS} = +12$ V if one assumes continuous DC Gate-Source bias of $V_{GS} = +12$ V at T = 175 °C for 10 years at a defect level of 1 Part Per Million (PPM). We will demonstrate that if we take into account MOSFET device lifetime as dictated by the Automotive Electronics Council (AEC Q101) mission profile, then devices can be rated higher to $V_{GS} = +14.7$ V at T = 175 °C for the same PPM level (1 PPM). The application of the methodology for establishing the oxide thickness, t_{ox}, for any required voltage rating, is discussed.

1. Introduction

The mechanism of dielectric breakdown in SiO_2 dielectrics has been studied extensively for many decades and several methodologies for reliability projections have been published. However, the vast majority of the current literature is on thin oxides (<11 nm) and there is very little in regards to reliability of thick oxides [1,2], despite the fact that thick oxides (>20 nm) are still essential for power MOSFETs. In addition, to the best of our knowledge, there is virtually nothing in the literature on the reliability of SiO_2 in trench MOSFETs, as usually the test structures for reliability studies are either simple MOS capacitors or DMOS devices.

In order to infer gate oxide lifetime for device normal operating conditions, results from accelerated reliability testing need to be obtained and in turn extrapolated to use conditions through the use of field and temperature dependent models, commonly referred to in the literature as the thermo-chemical "E model" [3] or "1/E" model [4]. In this work we will adopt the "E-model" as this is the model recommended by the "Automotive Electronics Council" (AEC) in their JESD22A-108 document for oxide lifetime prediction. Through the use of the "E-Model" one can transform stress conditions to use conditions via experimentally derived acceleration factors; activation energy (E_a) and field acceleration parameter (γ).

At this point we would also like to highlight that the most common difficulty with gate oxide reliability studies for MOSFETs, is that it is very time consuming for one to acquire Time Dependent Dielectric Breakdown (TDDB) data. The aim of this work was to also develop a novel experimental set up with which one can stress trench MOSFET devices in parallel and as such reduce the time for the acquisition of TDDB data considerably. The advantage of our approach is that we use actual experimental data on trench devices rather than relying on generic data on activation energies (E_a) and field acceleration parameters (γ) from the literature.

2. Experimental procedure

Devices under test (DUT) are 1.5 um pitch vertical trench N channel MOSFETs packaged in a Power SO8 package as in Fig. 1. The total gate oxide area is 1.45 mm^2 and consists of gate oxide along the trench walls and on the bottom of the trenches. Constant voltage stress (CVS) is carried out in the trench MOSFETs of Fig. 1 for positive gate-source voltages, $+V_{GS}$, for various oxide thicknesses, t_{ox}, ranging from 33 nm to 41 nm at different temperatures, T °C, using our experimental set up as illustrated in Fig. 2. Because of the topology of the N channel trench MOSFET during positive bias stress the device is both in accumulation and inversion as in Fig. 1.

On a PCB, ten DUTs are mounted, and gate to source voltage, V_{GS}, is applied from a power supply unit (PSU) through a 10 KΩ resistor to each device. The cumulative gate to source, I_{GSS}, current of the ten DUTs is recorded as a function of time. The failure for a single DUT is defined

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http://dx.doi.org/10.1016/j.microrel.2015.11.021
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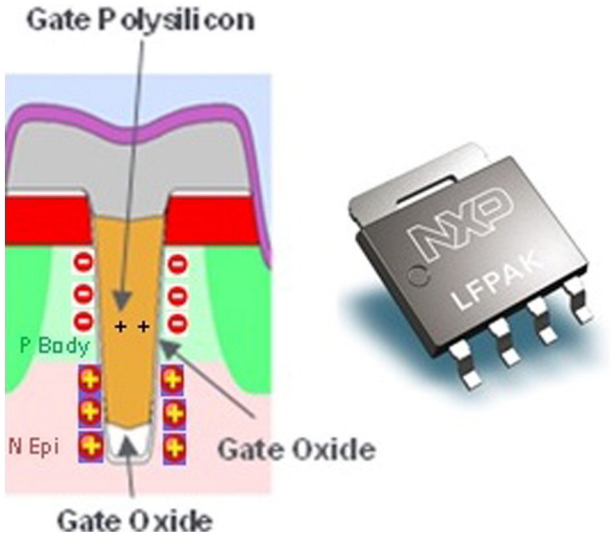

Fig. 1. Structure of an N-channel vertical trench MOSFET (left) packaged on an NXP Power SO8 package (Right). A positive bias at the polysilicon gate results in both inversion (⊖) (on the PBody side) and accumulation (⊕) (at the bottom of the trench which protrudes into the N Epi).

in time as jump of I_{GSS} of 1–3 mA. 4 PCB boards are connected to 4 individual PSUs and are all put in a single furnace; in essence we perform CVS, on simultaneously 40 DUTs at a single furnace temperature, T °C and at a single gate oxide field $E_{ox} = V_{GS}/t_{ox}$ (MV/cm) for all 40 DUTs. In our calculation of E_{ox}, we do not take into account polysilicon depletion effects (as we utilize thick oxides 33 nm–41 nm) or the work function difference between the polysilicon and the Pbody of the MOSFET.

By using the experimental set up of Fig. 2 we obtain TDDB data as in Fig. 3. In this particular example of Fig. 3, 40 trench devices with $t_{ox} =$ 38 nm were all stressed at a constant value of $V_{GS} = 30.5$ V ($E_{ox} =$ 8.03 MV/cm) and at T = 150 °C. The Y-axis represents the cumulative I_{GSS} current (i.e., the cumulative current through the gate oxide) for all 40 devices. As mentioned previously each "jump" in current indicates failure of a DUT in time; in the graph of Fig. 3, the "weakest" MOSFET fails at a time to breakdown, t_{BD}, of 285 h whereas the "strongest" fails at t_{BD} 1340 h. With the experimental set up of Fig. 3 we can produce a distribution of t_{BD} for 40 devices for any given pair of E_{ox} (MV/cm), T °C.

3. Results and discussions

3.1. Weibull plots of t_{BD} distribution, acceleration parameters

In Fig. 4, t_{BD} data for various pairs of E_{ox} (MV/cm), T °C stress, have been fitted to Weibull cumulative probability plots at a 65% confidence interval. In their well cited paper in the gate oxide reliability literature Hu et al. [5] have demonstrated that in the E-model for oxide lifetime prediction the time to breakdown of an oxide is given by:

$$t_{BD} = A_o \exp\left(\frac{E_a}{K_B T}\right) \exp(-\gamma E_{ox}) \quad (1)$$

where:

γ is the field acceleration parameter and is given by $\gamma = -\frac{\partial(\ln t_{BD})}{\partial(E_{ox})}$; γ is dependent on temperature as

$$\gamma = A + B\left(\frac{1}{T}\right) \quad (2)$$

E_a is the activation energy and is given by $E_a = K_B \frac{\partial(\ln t_{BD})}{\partial(1/T)}$; E_a is dependent of E_{ox} as

$$E_a = \alpha E_{ox} + \beta. \quad (3)$$

From Eqs. (2) and (3) and from the experimental data of Fig. 4, the field acceleration parameter (γ) has been derived as a function of temperature for the 4 different temperatures in our experiments (T = 125 °C, 150 °C, 175 °C, 200 °C). A graph of γ vs 1/T (K) is illustrated in Fig. 5. In a similar manner the activation energy, E_a, is plotted vs E_{ox} as in Fig. 6. Our results for both the activation energy and field acceleration parameters are in reasonably good agreement with the ones reported in literature for similar oxide thicknesses, [6,7].

For a similar E_{ox} stress regime to our own (6 MV/cm < E_{ox} < 10 MV/cm), McPherson et al. [6] report an activation energy of 0.85 eV with no strong field dependence. In our case E_a is fairly constant at 0.8 eV for E_{ox} < 8.8 MV/cm however for E_{ox} > 8.8 MV/cm E_a rapidly decreases with oxide field. We believe that this is because in our trench MOSFETs an oxide field of magnitude $E_{ox} = 8.8$ MV/cm, marks the onset of gate oxide avalanche, so we are no longer in the regime of the oxide "wear-out" phase but on the phase were destruction of the oxide occurs due to an avalanche multiplication effect. This onset of the avalanche region is also visible on Fig. 7, where gate current I_{GSS} is plotted versus V_{GS} for a MOSFET with 35 nm gate oxide. As evident from Fig. 7, one can distinguish three regions on the I_{GSS} vs V_{GS} graph. In Region I there is no current flowing through the gate oxide and only after $V_{GS} = 20$ V ($E_{ox} = 6$ MV/cm) (Region II) we get FN tunnelling through the oxide. For E_{ox} > 8.85 MV/cm ($V_{GS} = 31$ V) we observe an extremely steep increase in current. A subsequent I_{GSS} vs V_{GSS} reveals that the device is gate source "Short", i.e. the gate oxide has been destroyed. Similar I_{GSS} vs V_{GS} sweeps for other oxide thicknesses followed the exact same trend, that is a destruction of the oxide (observed as a steep increase in current) for $V_{GS} = V_{BD} \sim 1$ V/nm. In regards to field acceleration parameter γ, we report a range of 2–6 cm/MV for temperatures 125 °C < T < 200 °C which is in fairly good agreement with what Kimura [7] has previously reported.

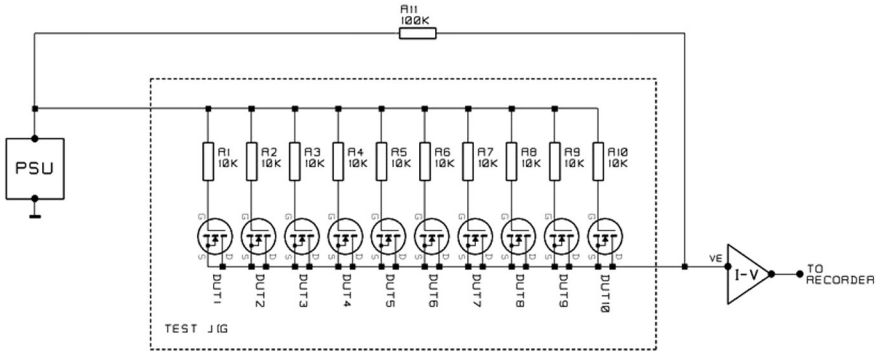

Fig. 2. Illustration of the experimental set up used. 10 DUT are PCB mounted and V_{GS} is applied from a power supply unit (PSU) through a 10 KO resistor for each device. The cumulative Igs current of the 10 DUT is recorded as a function of time. The failure for a DUT is defined in time as a jump of Igs of ~1–3 mA. 4 boards connected to 4 PSU are put in a furnace (40 devices).

Please cite this article as: E. Efthymiou, et al., A methodology for projecting SiO2 thick gate oxide reliability on trench power MOSFETs and its application on MOSFETs VGS rating, Microelectronics Reliability (2015), http://dx.doi.org/10.1016/j.microrel.2015.11.021