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Invited paper

The impact on power semiconductor device operation due to local electric field alterations in the planar junction termination

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ABSTRACT

In this paper, we present and discuss simulation and experimental results obtained from investigating the impact of local alterations of the electric field profile in the power device planar junction termination region. Such local modifications are due to possible various extrinsic causes (manufacturing, operational or environmental) and are shown to have a critical influence on the device voltage blocking capability and reliability. The results point towards junction termination sensitivity to locally modified fields especially under voltage switching conditions due to higher leakage current densities in the modified area compared to the rest of the JT region.

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1. Introduction

In the past few decades, the power electronics revolution has opened up a wide range of possibilities in terms of controlling the way electrical energy is transported and used. At the heart of this revolution are power semiconductor devices which are in general terms covering an ever increasing number of applications and are experiencing continuous improvements in their performance and reliability. The main technology development trend in power devices has always been focused on increasing the power ratings while also improving the overall device performance in terms of reduced losses, increased robustness, better controllability and in particular, *reliable behaviour under normal and stress/fault operational conditions*. High voltage power semiconductors differ from their low voltage counterparts in a number of structural and design aspects as shown in Fig. 1. In addition to the active area region which basically defines the device concept "diode, Thyristor, MOSFET, IGBT, etc." [1], they include:

1- the bulk region having a wide and low doped base "drift" layer to support the electric field required for the high voltage ratings
2- the junction termination (JT) region to shape the pn junction edge and surface profile for obtaining a controlled electric field distribution and the maximum possible reverse voltage blocking capability.

In relation to the topic of this paper, the JT region plays a critical role in all device operational modes except during the on-state conduction. During static blocking (reverse bias), turn-on and turn-off switching and under special overload and fault protection conditions, high voltages are applied across the device. Therefore, the design and protection of the JT region play a very important role in ensuring uniform and controlled electric field profiles for maintaining breakdown voltage capability under all operational conditions.

The main target of this work was to investigate the impact of possible local electric field modifications in planar JT regions on the device blocking capability. Planar JT designs are employed for the majority of modern power semiconductors such as IGBTs or diodes and also for silicon carbide based devices including MOSFETs and diodes. It is important to point out that the findings can also be applicable to non-planar JT concepts as described below.

2. Power device junction termination and passivation

Over the past few decades and in line with the advances made in power semiconductor devices and materials, a wide range of junction termination and passivation concepts have been proposed, developed and implemented. In brief, two main design principles have been employed as follows [2]:

1- mesa/bevel edge etching which is widely used in bipolar devices such as diodes and thyristors [3]
2- planar designs including floating guard rings (GR) [4] with or without field plates or junction termination extension (JTE) designs [5]. GR and JTE designs are compatible with MOS based planar device structures such as MOSFETs or IGBTs as well as for chip diodes.

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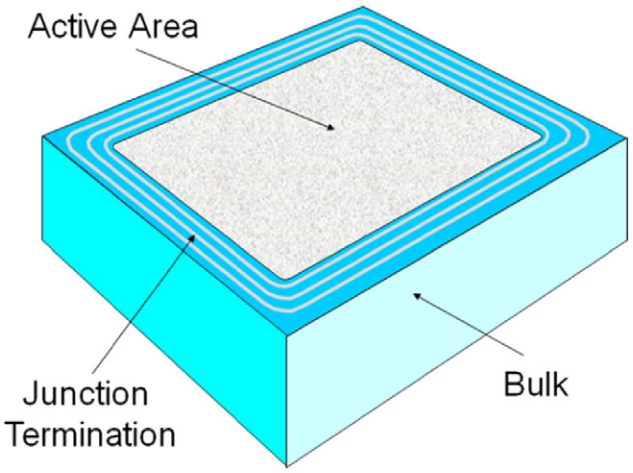

Fig. 1. Power semiconductor planar device basic structure.

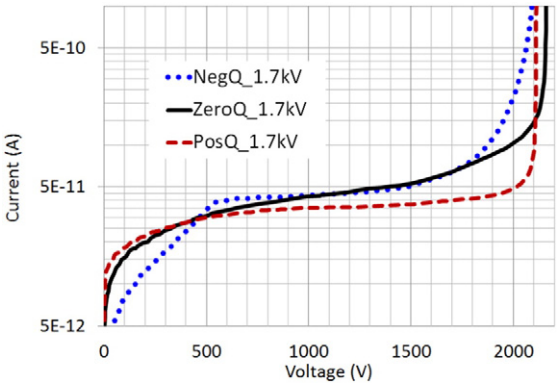

Fig. 3. Static blocking simulation results for a 2D 1.7 kV IGBT design at 25 °C with VLD JT having positive, zero and negative surface charges (device area is 8.68E−06 cm^2).

Furthermore, a number of different passivation and protection layers are utilized depending on the junction termination design requirements [6]. Such layers include insulating layers (silicon oxide or nitride), semi-insulating layers (SIPOS or diamond-like-carbon) and protective layers (polyimide or rubber) to name a few [7].

In principle, the junction termination and passivation concept can be subdivided in terms of design and functionality as follows:

1- the junction termination design in the semiconductor bulk: which controls the edge curvature of the pn junction and hence the shape of the electric field towards the surface. It is also desirable by design to ensure that any high electric fields at the junction periphery are located as remote as possible from the semiconductor surface. Apart from the highly doped regions, the JT design also includes an extension zone or region to allow the spreading of the electric field towards the outer edge of the device.
2- the first passivation layer: which forms the interface to the semiconductor surface for defining the surface charge Q_{ss} levels responsible for the electric field spreading in lower doped regions while achieving low peak electric field levels. Conducting field plates and semi-insulating layers are normally used to help further spread the electric field at pn junction periphery regions. In addition, the semi-insulating layers also aid in providing fixed interfacial charges at the surface while providing a path for any possible trap charges accumulating at the semiconductor interface.
3- the top passivation layers: which are mainly responsible for protecting the junction termination region from any potential external mechanical damage or contamination which could alter the electric potential and field distributions in the junction termination. These layers also provide high insulation for ensuring that no premature voltage breakdown occurs at the surface of the device due to flashovers.

In addition, further protection is usually provided when the devices are finally encapsulated in a package [8]. Hermetic modules provide normally close to ideal protection from external environmental conditions for very high reliability applications while insulated modules offer a number of additional protection layers such as polyimide and silicone gel. The above description is illustrated in Fig. 2 for a typical JTE structure referred to as variable lateral doping (VLD) [5] employed for an IGBT chip.

With major advancements in TCAD power device simulation tools, junction termination designs are optimized today while taking into account many variables to achieve the maximum blocking capability per design. In addition, transition zones and interactions between the junction termination and active area regions during switching transients are perfected to achieve high robustness with respect to the device safe-operation-area (SOA). The optimization also takes into account a certain tolerance for possible variations in the fixed surface charge in the region between 1e11 and 1e12/cm^3 considering both positive and negative charge polarities [9].

To illustrate such effects, Fig. 3 shows the 2D blocking simulation results at 25 °C for a 1.7 kV IGBT design with VLD junction termination for a 5e11/cm^3 positive, a 5e11/cm^3 negative and a zero surface charge.

Fig. 4 shows the simulated cross sections for the electric field distribution at 1700 V and Fig. 5 shows the corresponding electric field distribution plots. The results display how, as a result of Gauss law, the surface charge levels can alter the shape of the electric field profile and the position of its peak while providing different voltage blocking behaviours and still satisfying the target blocking capability of the device. Nevertheless, the negative surface charge in this case results in the extension of the field to the edge of the chip where in reality this

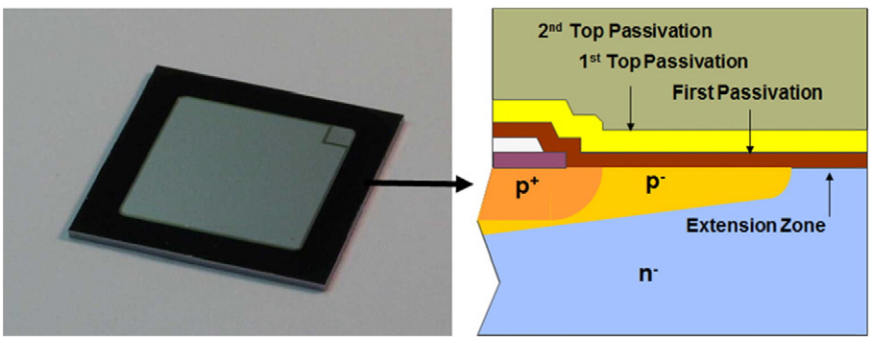

Fig. 2. Typical planar junction termination cross section for an IGBT device with VLD junction termination.

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