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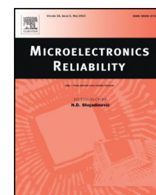

Requirements in power cycling for precise lifetime estimation

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ABSTRACT

This paper discusses power cycling as a method to evaluate the reliability of interconnections in power electronic devices. While the approach proved a reliable tool for investigating the potential of improvement for alternative interconnect technologies and rejecting design flaws, precise estimations about lifetime in the field are still challenging. Many questions are still in discussion, such as ultra-high cycle fatigue, applicability of Miner's rule, or the influence of on-time and cross-effects with mechanical shocks or humidity. This leaves application engineers with a blurred safety margin. In the following basic considerations of power cycling are described. The introduction shows two applications with different load profiles. Section 2 explains methods of temperature measurement. In Section 3 theoretical requirements for measurement accuracy are given, the obstacle minimal measurement delay and possible workarounds are evaluated. Finally aging effects and their acceleration in different devices are discussed in Section 4. In the conclusion suggestions for power cycling methods and a revision of the end-of-life criteria are made.

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1. Introduction

Reliability in terms of power electronic devices focuses on the endurance of a device to maintain its functionality as a switch or valve, more precisely to block its specified voltage when turned off, conduct the nominal current when turned on and handle switching dynamics. Demands for reliability are defined by application. In hybrid electrical vehicle (HEV) applications for example, short and relatively high active power cycles are superimposed with high passive cycles, caused by minimized or shared – with combustion engine – cooling circuits [1,2]. Where active cycles have their cause in changes of the devices power losses and passive cycles are caused by external sources, such as ambient temperature or external heat sources. An example of passive cycles of more than 150 K occurring after starting a system at temperatures around 0 °C is given in Fig. 1, while most active cycles happen at temperature swings ΔT_j less than 50 K and short on-time t_{on} of less than 5 s. In wind power applications, however, temperature changes are less dynamic and higher temperature swings correlate to longer on-times, contrary lifetimes longer than 20 years are demanded (see Fig. 2).

Power cycling tests are typically highly accelerated tests, with on-times in the range of a few seconds to address chip close connections or a few seconds to some minutes to stress outer layers such as the system solder or thermal interface materials of power modules. In the process, the joints are typically stressed with higher temperature swings and higher temperature gradients than occurring in the field leading to a comparable cycle fatigue. This enables testing until end-of-life within several weeks up to several months. Temperature swings ΔT_j below 50 K have been rarely investigated and published in the past 20 years, see Fig. 3 taken from [4].

2. Temperature measurement

JEDEC defines the virtual-junction temperature T_{vj} being “A temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behavior of the semiconductor device.” [5]. Methods to use the chip itself as temperature sensor using temperature sensitive electrical parameters (TSEP) have been investigated and applied for more than fifty years [6].

In power electronics, the temperature dependent voltage drop at junction(s) at low current densities is the most widely accepted and investigated method. With the IGBT being the major subject of power cycling activities, the term V_{CE}(T)-method is used. For pn-junctions in silicon the voltage change by temperature is typically around −2 mV/K. Linear characteristics are found up to 1700 V nominal voltage. High voltage devices may inhibit non-linear characteristics, due to a contribution of the wide low doped base, as the example for a 6.5 kV IGBT in Fig. 4 shows. It can further be seen that an error of 5% in measurement current leads to a measurement error of 1.7 K at 140 °C and 100 mA measurement current.

In former investigations the measured virtual junction temperature T_{vj} was found to be the upper third value in between maximal and minimal temperature on the chip surface (simplified example: $T_{vj} = 150$ °C, $T_{max} = 160$ °C, $T_{min} = 130$ °C), when heating an IGBT by nominal

Abbreviation: NTC, negative temperature coefficient of a physical property; PTC, positive temperature coefficient of a physical property; HEV, hybrid electric vehicle.

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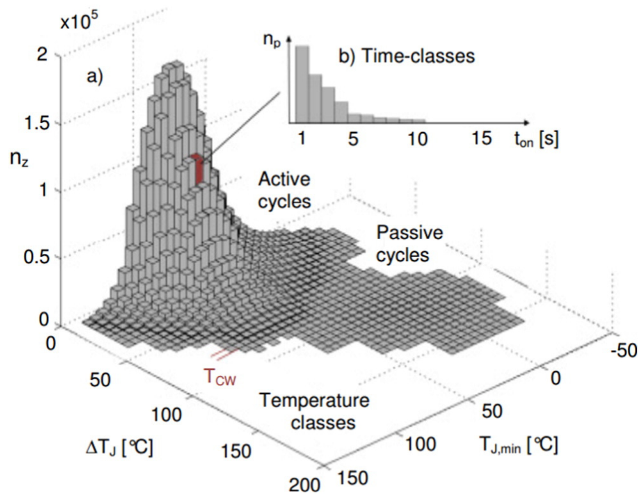

Fig. 1. Temperature swings ΔT_j of IGBTs in a HEV-application taken from [2], majority of cycles is below 50 K, majority of cycles with 20 K temperature swing in the range of a few seconds hints to highly dynamic shift of work points in drives applications, n_z is the total number of cycles at the given T_{jmin} and ΔT_j, each n_z is the sum of n_p for number of cycles listed in classes of on-time t_{on}.

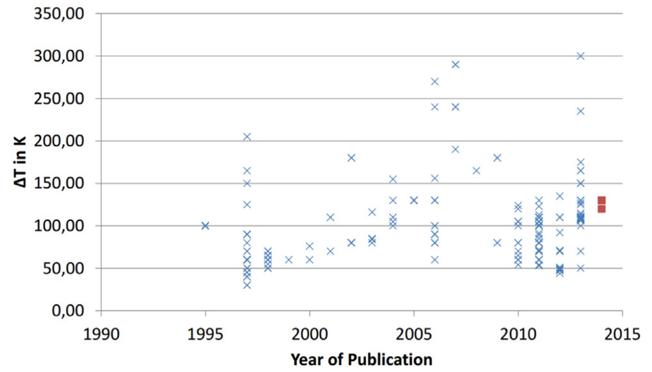

Fig. 3. Temperature swing ΔT_j of published power cycling tests by year of publication, taken from [4].

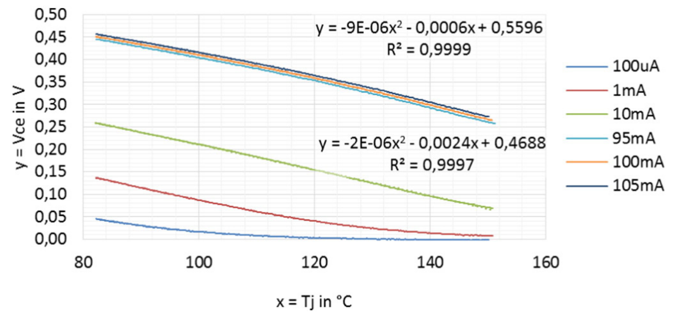

Fig. 4. $V_{CE}(T_j)$-calibration curves of a 6.5 kV 200 A IGBT-module, with different measurement current I_{meas},(own measurements).

current and reaching almost steady state conditions [7,8]. For standard module technology, where the biggest thermal time constant of the thermal impedance lies at around 1 s — steady state conditions are almost reached after just a few seconds and temperature distribution across the chip does not vary significantly, appropriate cooling provided. However, T_{vj} as measured by the $V_{CE}(T)$-method alone is not a sufficient measure for reliability when investigating short on-time of less than 0.5 s, see Figs. 5 and 6. The difference to the maximal temperature lies at around 5–10 K. The minimal temperature in the corner is about 50 K lower instead, thus changing the position of maximal induced stress. Thereby, the origin of crack growth changes from the edge for lower power density to the chip center at higher power density. The basis for a new crack growth model respecting such effects was developed in the project “Zuverlässige Lötverbindungen für die Leistungselektronik in regenerativen Energiesystemen” (Reliable solder connections for power electronics in renewable energy systems) funded by the German Research Association DFG. Applying the $V_{CE}(T)$-method under inverter conditions is possible and was demonstrated in [9,10].

3. Measurement accuracy

In available lifetime models the virtual junction temperature T_{vj} is of great importance in the design of power electronic systems as the temperature swing ΔT_j influences lifetime with a power of −4.4 up to −5, as described by lifetime models [11–13]. Therefore, it is the most critical parameter influencing the accuracy of results in power cycling tests. For low temperature cycles ΔT_j of 50 K, an accuracy of 1 K is needed to stay within the 10% tolerance of estimated cycles to failure according to the CIPS 2008 model. Typically, the achieved measurement uncertainty after heating with nominal current is in the range of around 3–8 K for silicon and around 5–10 K for SiC devices. It varies significantly with the device under test itself, its voltage class, uni- or bipolar, semiconductor material etc., as well as the temperature and load power density.

The importance of a precise ΔT_j-measurement in power cycling becomes visible when discussing the CIPS2008 model (Eq. (1)) [12] with parameters for typical test conditions according to, Table 1, found in [14]. There, the exponent to describe the dependency of ΔT_j on the lifetime is $ß_1 = -4.416$. Table 2 shows an example where all test conditions are kept constant and only ΔT_j varies. Assuming a desired accuracy of the test result lifetime N_f of less than 20%, the allowable measurement error $\Delta T_{j,error}$ drops from 6 K at $\Delta T_j = 150$ K down to 1 K at $\Delta T_j = 30$ K. This makes testing of high cycle fatigue with short

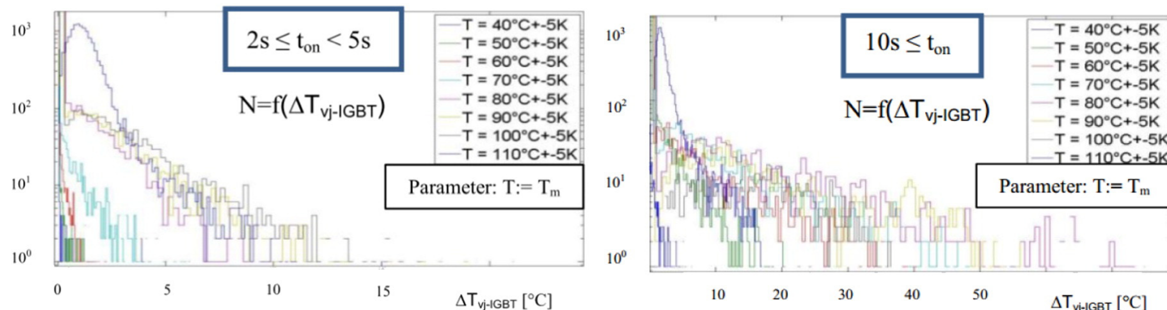

Fig. 2. Extracted temperature cycles from operating an offshore wind power application during one week taken from [3], for on-time $t_{on} < 5$ s temperature swings stay below 15 K, higher ΔT_j is observed for $t_{on} > 10$s only.

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