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A simple 1-D finite elements approach to model the effect of PCB in electronic assemblies

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ABSTRACT

In this paper, a simple method to describe the effect of Printed Circuit Board (PCB) and environment on the thermal behavior of packaged devices is addressed. This approach aims at exploiting the benefit of compact thermal models, which are necessarily one-dimensional, together with the advantage of Finite Element (FE) modeling, which retains all the three-dimensional geometrical details, only in the regions of the model that must be accurately described. The main focus is on correct modeling of long power pulses for subsequent electro-thermal and thermo-mechanical analysis at chip level.

1. Introduction

In the field of automotive electronics, achieving strong device reliability is a primary requirement. Operating typical automotive loads, such as light bulbs or servo-motors, represent a strong thermal stress for the device itself due to high inrush current, long turn-off times, and high inductances these loads feature. As a result, switching these loads implies high switching losses, long turn-on and turn-off transients, and strong overheating. The switches will be cycled from thousand to million times and the corresponding power cycles will induce thermo-mechanical degradation, eventually leading to electrical failure. It is thus necessary to correctly model such power cycles to improve device reliability and understand failure mechanisms, and in particular an accurate thermal model is the first step to draw all the subsequent electro-thermal and thermo-mechanical conclusions.

From a modeling point of view, there is always a trade-off between (a) the duration of the power dissipation pulse and (b) the level of detail necessary to capture the important thermal effects. A typical electronic switch for low voltage automotive applications is shown in Fig. 1. In case of short pulses (10 μs ÷ 1 ms) it is enough to model the device down to the die attach level, neglecting the effect of package and PCB on the overall thermal behavior, because the heat wave does not reach the latter domains.

In case of long pulses (duration >1 s), the situation is reversed: the internal structure of the device can be simplified while the correct modeling of pins, solder joints, and PCB is important.

However, this simplification approach has some limits, since the device is assumed to be mechanically perfect and always operating in a thermally stable region. In case of automotive MOSFETs, they can indeed be operated below the Temperature Compensation Point (TCP), that is, under unstable regime [1]. In case of long pulses, the PCB should be included in the electro-thermal model, as well as a detailed model of the packaged device itself. This kind of problems where in the same model it is necessary to describe tiny and wide features at the same time (e.g., bonding wires, whose diameter is on the order of tens of μm, and PCB, with typical dimension on the order of centimeters) is always a challenging engineering topic.

While different approaches are available [2,3] for solving these problems, a simple alternative method is presented where, basically, the PCB is simplified in order to reduce the Degrees of Freedom (DoFs) of the overall simulation.

In the next sections the basics of the method are explained and two case studies are provided.

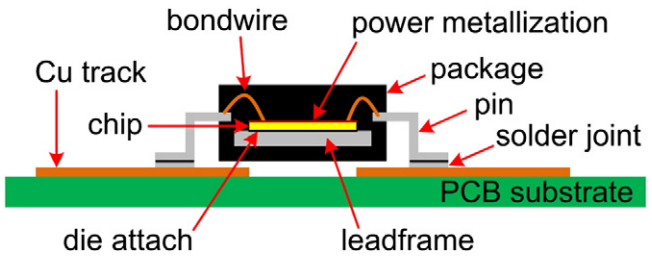

Fig. 1. A schematic view of a packaged device mounted on PCB with indication of some typically modeled features.

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2. The simplification approach

Lumped Element Models (LEMs) are well known in literature and here will be briefly recalled. These models rely on the formal analogy between Fourier thermal equation and electrical circuit equations, thus allowing the description of a thermal system by means of *R–C* networks where thermal resistances and thermal capacitances model the heat flow path. Physics-based LEMs are useful since they can capture the actual heat flow in the structure, but generally they necessitate of many elements [4]; on the other hand, empirical models [5] (based on Foster and Cauer networks) are very quick to be solved but, except for multilayer stacks, there is no physical link with the structure they are describing.

The approach here explained aims at merging the benefits of LEMs with the advantages in terms of geometric description provided by FE models. The fundamental assumption is that heat propagation through the contact surfaces between pin, or its solder joint, and PCB can be modeled in a quasi-1D way. As a rule of practice, each solder joint at a pin end corresponds to a contact surface as shown in Fig. 2.

A given heat flux P_{S_i} [W] will flow across the *i*-th contact surface, being T_{S_i} the surface-averaged temperature of the contact surface itself [K]. The thermal impedance at the *i*-th contact surface Z_{th_i} is calculated as follows:

$$Z_{th_i} = \frac{T_{S_i} - T_{amb}}{P_{S_i}} \quad [\mathrm{K/W}] \tag{1}$$

Eq. (1) describes the thermal behavior at the contact surface assuming 1D heat transfer. The reference temperature T_{amb} is that of the ambient.

The next step is to obtain a Cauer LE model which fits the above thermal impedance response at the contact surface, as described in Section 2.1

Once the set of (R_m, C_m) values for the Cauer representation is obtained, the LE model is back-transformed into its equivalent FE model on the basis of geometric considerations. For each *RC* stage, a fictitious layer of a stack with adiabatic lateral walls in the FE model will be generated. Material properties are determined in order to ensure the same 1D thermal impedance response for both LE and FE models.

Fig. 3 shows the above-described process. Assuming a contact surface A_i, the thermal impedance at its location is calculated and the equivalent Cauer network is obtained. Then, if *n* stages are found (for instance $n = 3$ in Fig. 3), a stack of *n* materials m_1, m_2, … m_n will be generated in the FE model. It is important to note that the bottom of the stack is fixed at $T = T_{amb}$, and that this stack of fictitious materials includes also the effect of the boundary conditions set in the original model around the PCB.

As shown in Fig. 3, the cross-sectional area on the *xy* plane is fixed by the contact surface, while the thickness of each layer is chosen

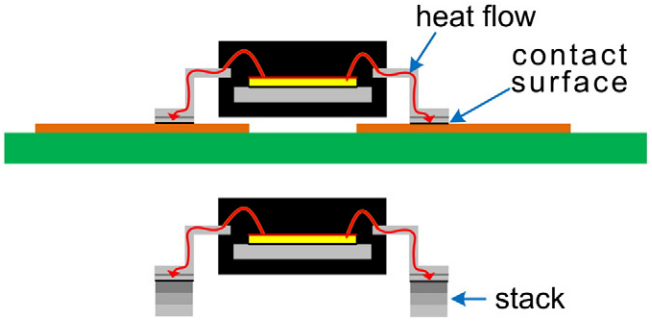

Fig. 2. Cross-sectional view of heat flow through the contact surfaces in the full model (top) and in a simplified model where an equivalent stack of different materials is determined (bottom).

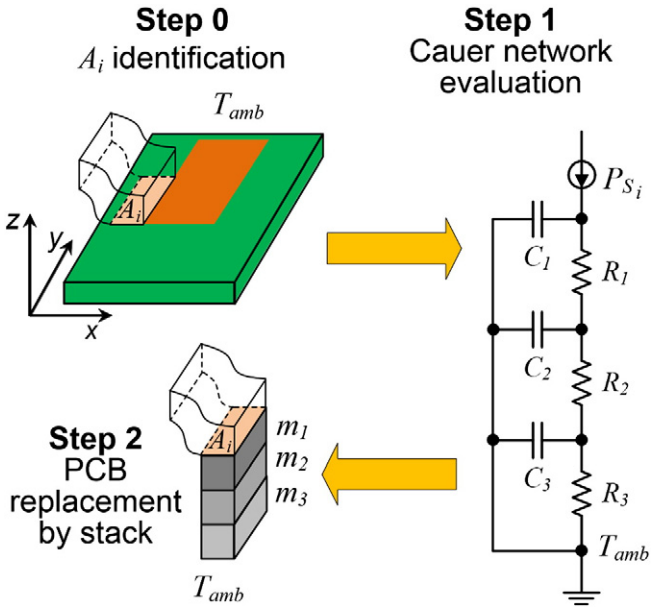

Fig. 3. Graphical representation of the simplification method.

considering mesh constrains. Meshing is eased when adjacent volumes feature comparable thickness.

Clearly, this equivalent model cannot be classified as a Boundary Condition Independent (BCI) model [6,7]: if the boundary conditions change, the simplification process must be re-performed.

2.1. Determination of the Cauer network

The determination of the Cauer network is needed in order to obtain the equivalent stacks replacing the PCB under the pins in the simplified FE model. Here, the procedure for one contact surface is explained using a reference model with a D2PAK MOSFET mounted on a PCB with a standard FR4 substrate (thickness 1.6 mm, 1 oz copper).

The main idea is to determine the Cauer networks for every contact surface (e.g. gate, drain and source) by applying a stepped heat-flux waveform at each A_i, keeping all the other contacts thermally insulated. It is firstly necessary to obtain the corresponding Foster networks:

$$\forall i \; Z_{th_i}(t) = \left. \frac{T_{S_i}(t) - T_{amb}}{P \cdot u(t)} \right|_{P_{S_j} = 0 \; \forall \; j \neq i} \tag{2}$$

where $u(t)$ is the unit step function, *P* is the amplitude of the stepped heat flow ($P_{S_i}(t) = P \cdot u(t)$).

The simplified model obtained in such a way did not provide satisfactory results, because it neglects the mutual thermal influence between each A_i.

A second attempt consisted in applying a stepped heat-flux waveform to every contact surface at the same time:

$$\forall i \; Z_{th_i}(t) = \frac{T_{S_i}(t) - T_{amb}}{P \cdot u(t)} \tag{3}$$

This approach resulted in unsatisfactory results too, since the mutual influence between each A_i couple is in general different from the others, due to different copper track dimensions, different area sections, and so on.

It turns out that none of the above mentioned methods produces reliable approximations. Thus, in order to calculate the Foster network to transform into Cauer form, the best way to take into account (a) the different paths (magnitudes and delays) between the chip and the contact surfaces, and (b) the $P_{S_i}(t)$ interactions in the PCB, is to