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Trapping and reliability issues in GaN-based MIS HEMTs with partially recessed gate

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ABSTRACT

This paper reports an extensive analysis of the trapping and reliability issues in AlGaN/GaN metal insulator semiconductor (MIS) high electron mobility transistors (HEMTs). The study was carried out on three sets of devices with different gate insulators, namely PEALD SiN, RTCVD SiN and ALD Al_2O_3. Based on combined dc, pulsed and transient measurements we demonstrate the following: (i) the material/deposition technique used for the gate dielectric can significantly influence the main dc parameters (threshold current, subthreshold slope, gate leakage) and the current collapse; and (ii) current collapse is mainly due to a threshold voltage shift, which is ascribed to the trapping of electrons at the gate insulator and/or at the AlGaN/insulator interface. The threshold voltage shift (induced by a given quiescent bias) is directly correlated to the leakage current injected from the gate; this demonstrates the importance of reducing gate leakage for improving the dynamic performance of the devices. (iii) Frequency-dependent capacitance–voltage (C–V) measurements demonstrate that optimized dielectric allow to lower the threshold-voltage hysteresis, the frequency dependent capacitance dispersion, and the conductive losses under forward-bias. (iv) The material/deposition technique has a significant impact on device robustness against gate positive bias stress. Time to failure is Weibull-distributed with a beta factor not significantly influenced by the properties of the gate insulator.

The results presented within this paper provide an up-to-date overview of the main advantages and limitations of GaN-based MIS HEMTs for power applications, on the related characterization techniques and on the possible strategies for improving device performance and reliability.

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1. Introduction

Thanks to the extensive efforts carried out over the last decade, the technology of nitride-based transistors has shown impressive advancements. Gallium nitride has several advantages compared to more conventional semiconductors like GaAs and silicon, namely: (i) GaN-based transistors can reach a very high maximum oscillation frequency (>200–300 GHz, [1]), thanks to the high electric field saturation velocity and to the low parasitic capacitance; and (ii) GaN has a wide bandgap of 3.4 eV; as a consequence, GaN-based transistors can be operated at high temperature levels (>400 °C) [2]. This property has direct advantages at system level, since it allows one to reduce the size/weight of the heat sinks used for GaN transistors. (iii) GaN has an extremely high breakdown field (3.3 MV/cm, compared to Si and GaAs that are below 1 MV/cm) [3]; GaN transistors can therefore have breakdown voltages in the kV range, thus being suitable for application in power electronics [4]. (iv) Finally, the use of an AlGaN/GaN heterostructure results in the generation of a high mobility electron gas; as a consequence, GaN-based HEMTs can have a very low on-resistance, and a very low Ron·Qg product (smaller than 1 nC·Ω), with a significant lowering of the switching losses of transistors, if compared to conventional Si devices.

Thanks to the properties listed above, GaN-based transistors represent almost ideal devices for the fabrication of high efficiency power converters, to be operated in the 600–1200 V range. Over the last few years several research groups have focused on the development of metal-insulator-semiconductor (MIS) HEMTs [5]: a thin (5–15 nm) insulating layer is deposited on the AlGaN before the deposition of the gate contact. This has a beneficial effect in terms of leakage, since it permits one to significantly reduce the gate current when the device is biased both in forward- and in reverse-bias conditions. In several cases, the AlGaN layer is partially (MIS-HEMT) or totally (MOS) recessed in order to improve device performance. Several dielectrics have been proposed as gate insulators [6,7], including SiN [8], Al_2O_3 [9], SiO_2 [10], HfO_2 [11], and TiO_2 [12]. In most of the cases these dielectrics are deposited by chemical vapor deposition (CVD, as in the case of SiN) or by atomic layer deposition (ALD, as in the case of Al_2O_3).

Recent studies demonstrated that the gate insulator can be a critical element in terms of device performance and reliability. Depending on the deposition method [13] and material quality, the dielectric/AlGaN

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interface may have several defects that can favor threshold voltage (V_{th}) shift and hysteresis.

Several methods have been proposed/used for the analysis of the trapping processes related to the gate insulator in MIS-HEMTs: admittance measurements [14], photoassisted C–V measurements [15], and dynamic conductance/transconductance analysis [16]. All these methods – which are similar to those adopted in conventional MOS devices – provide information on the density and energy distribution of the interface traps. However, recent studies [17] demonstrated that the effectiveness of capacitance/conductance methods is limited by the intrinsic frequency response of the gate stack: the presence of AlGaN may result in peaks of the conductance/frequency curves even without traps, and this may generate errors when analyzing the experimental data.

An effective method for investigating the trapping/detrapping mechanisms related to interface defects is represented by stress/recovery experiments; in these measurements, the V_{th} dynamics are analyzed by an oscilloscope during forward gate bias stress pulses. The results described in [18] demonstrate a broad distribution of the de-trapping time constants; this was explained by considering a distribution of capture cross section due to the disordered nature of oxide states, a distribution of tunneling distances between interface and border traps, or spatially distributed leakage paths in the AlGaN/GaN with varying leakage current (see [19] for details).

Another relevant issue of GaN-based MIS-HEMT is represented by the robustness of the gate insulator: recent studies [20–23] demonstrated that – similarly to MOS devices – GaN MIS-HEMT suffers from time-dependent breakdown and catastrophic failure.

Since there are several possible combinations of gate dielectric and deposition techniques that can be used for the fabrication of GaN HEMTs, it is important to compare different technologies in terms of performance, trapping and reliability. The aim of this paper is to present an extensive analysis of the dynamic performance and reliability of GaN-based MIS-HEMTs; three sets of devices with different gate insulators (RTCVD SiN, PEALD SiN and ALD Al_2O_3) and identical AlGaN/GaN heterostructures were used in this study. Based on combined dc, pulsed and transient measurements we demonstrate that: (i) the quality/properties of the gate insulator can significantly impact the dc and dynamic performance of the devices; (ii) in all the three sets of devices the dynamic V_{th} shift induced by positive gate bias is correlated to the leakage current flowing through the gate; (iii) stress/recovery experiments confirm the dynamic V_{th} shift induced by a positive gate bias and its dependence on the gate insulator; and (iv) constant voltage stress experiments indicate that the use of PEALD SiN may result in high device robustness. It further indicates that in all the sets of samples time to failure is Weibull-distributed with $\beta \approx 1.1–1.5$.

2. Experimental details

The analysis was carried out on metal-insulator-semiconductor (MIS) HEMTs grown on a 200 mm silicon substrate by metal organic chemical vapor deposition (MOCVD). The top structure consists in a 150 nm thick GaN channel layer with a partially recessed AlGaN layer. The thickness of the residual AlGaN is 3.7 nm. The ohmic metal stack consists of 5/100/60 nm Ti/Al/TiN, resulting in a contact resistance of 0.65 Ω mm. Three different gate insulators were used: wafer A, with a 15 nm SiN layer deposited by rapid thermal chemical vapor deposition (RTCVD); wafer B with a 15 nm SiN layer deposited by plasma enhanced atomic layer deposition (PEALD); and wafer C, with a 15 nm Al_2O_3 layer deposited by atomic layer deposition (ALD).

The electrical properties of the MIS gate-stacks were investigated by means of complementary current–voltage (I–V) and capacitance–voltage (C–V) measurements. The impact of different dielectrics on the dynamic performance of related MIS-HEMTs was investigated by submitting transistor structures to pulsed and transient measurements, that were carried out by a custom setup on devices with $W_G = 100$ μm and $L_{GD} = 5$ μm. Current–voltage curves (in this case I_D–V_G transfer characteristics) were executed by pulsing both gate and drain terminals from various quiescent bias point (V_{GS_Q}, V_{DS_Q}), in order to monitor the stability of the threshold-voltage and transconductance [24] (V_{GS_Q} and V_{DS_Q} represent the quiescent bias points on the gate and on the drain respectively); both negative and positive gate biases, were used. A pulse width of 1 μs with a duty cycle of 1% was applied.

Further information on charge-trapping and detrapping kinetics in the MIS gate stack was collected with stress and recovery transient measurements: devices were exposed to forward-bias stress for 1 ks, followed by a relaxation phase at (0 V;0 V). The threshold voltage shift kinetics was evaluated during both the stress and the relaxation phases by means of pulsed on-the-fly technique, already adopted by Lagger et al. in [19].

Finally, step- and constant-stress tests were performed to assess the long-term reliability of the tested MIS gate stacks, and to collect information on the related time-dependent breakdown mechanisms.

3. Results

3.1. Dc characterization

Fig. 1 shows the current–voltage (I–V) breakdown on devices with different gate insulators; the measurements were performed on devices with equal gate-source length (L_{GS}) and gate-drain length (L_{GD}) ($L_{GS} = L_{GD}$), by biasing the gate terminal with a positive increasing voltage while keeping drain and source terminals grounded (and thus evaluating the parallel of the gate-source and gate-drain diodes). Current–voltage curves indicate that the use of PEALD-SiN can significantly lower the gate leakage current with respect to the RTCVD SiN and ALD Al_2O_3: with a gate voltage of 5 V the PEALD-SiN structure demonstrates a leakage more than three orders of magnitude lower than both ALD-Al_2O_3 and RTCVD-SiN devices. The use of ALD Al_2O_3 gate insulator induces a slight improvement with respect to RTCVD SiN structures (less than one order of magnitude for gate voltage ranging from 4 V to 6 V).

Furthermore we can notice that both RTCVD and PEALD SiN structures demonstrate two different conduction regimes, depending on the gate voltage. The slope of the I–V curves shows a significant change when the gate bias (V_G) becomes higher than 8.7 V (10.7 V) for the RTCVD (PEALD) SiN devices. This indicates a change in the dominant conduction mechanism for high voltages. This effect is not observed in devices with Al_2O_3 gate insulator.

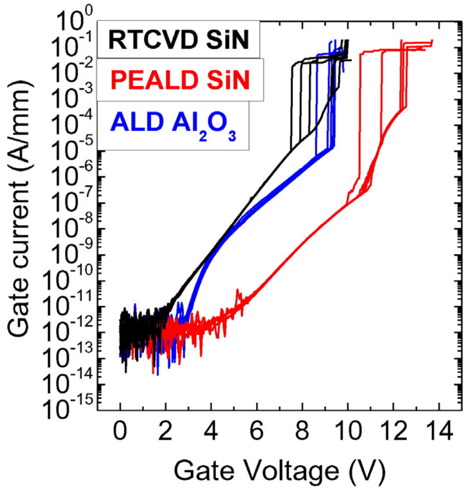

Fig. 1. Current–voltage breakdown measurements on devices with different gate insulators: RTCVD SiN (black line); PEALD SiN (red line); and ALD Al_2O_3 (blue line). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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