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Reliability of Diode-Integrated SiC Power MOSFET(DioMOS)

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ABSTRACT

Status of the reliability study on silicon carbide (SiC) power MOS transistors is presented. The SiC transistors studied are diode-integrated MOSFETs (DioMOS) in which a highly doped n-type epitaxial channel layer formed underneath the gate oxide acts as a reverse diode and thus an external Schottky barrier diode can be eliminated. The novel MOS device can reduce the total area of SiC leading to potentially lower cost as well as the size of the packaging. After summarizing the issues on reliability of conventional SiC MOS transistors, the improvements by the newly proposed DioMOS with blocking voltage of 1200 V are presented. The I–V characteristic of the integrated reverse diode is free from the degradation which is typically observed in conventional pn-junction-based body diode in SiC MOS transistors. The improved quality of the MOS gate in the DioMOS results in very stable threshold voltage within its variation less than 0.1 V even after 2000 h of serious gate voltage stresses of +25 V and −10 V at 150 °C. High temperature reverse bias test (HTRB) shows very stable off-state and gate leakage current up to 2000 h under the drain voltage of 1200 V at 150 °C. These results indicate that the presented DioMOS can be applied to practical switching systems free from the reliability issues.

1. Introduction

Silicon Carbide (SiC) is a wide bandgap semiconductor that is very suitable for power switching applications especially at high voltage and current. Technical breakthroughs on the crystal growth and the consequent development of the processing technologies have resulted in successful commercialization of SiC Schottky barrier diodes. SiC MOS transistors with superior performances to existing Si power transistors have also been demonstrated and thus wide spread use of SiC transistors in the near future would be expected with the establishment of the reliability. Although the performances in DC and/or switching of the reported SiC MOSFETs are sufficiently good, there remains an issue of high fabrication cost because of the inherently high cost of the SiC substrate. Thus establishment of good enough reliability with reduced fabrication cost is very critical for the widespread use of SiC MOS transistors. So far, diode-integrated MOSFET (DioMOS) has been proposed as a solution to reduce the area of SiC for practical switching by the integration of the reverse diode on to the transistor [1–4]. Here additionally formed n-type epitaxial channel layer serves current path for the reverse conduction in the DioMOS so that an external diode to flow the reverse current can be eliminated. Elimination of external diode leads to a reduction of the total number of devices in the system resulting in significant cost down. The DioMOS with satisfactorily good reliability would help the wide spread use of SiC power switching transistors.

In this paper, status of the reliability of the SiC DioMOS is summarized after reviewing the reliability issues of conventional SiC MOS transistors. With the help of channel diode avoiding current flow to the body diode that causes the degradation in conventional MOSFET, the DioMOS exhibits very stable characteristics at high temperature and under high drain voltage of 1200 V. This indicates that the DioMOS will greatly help the widespread use of SiC transistor taking advantage of the reduction of the total area of SiC contributing to reduce the total system cost.

2. Reliability issues of conventional SiC-MOSFET

SiC power transistors that have been widely investigated so far are vertical MOS (Metal-Oxide-Semiconductor) transistors. The structure as shown in Fig. 1 is identical with that of conventional Si power MOS transistors called DMOS (Double diffusion MOS). Issues of reliability in conventional SiC DMOS are also described in Fig. 1, of which the details are described below.

The most critical reliability issue of SiC MOFET so far has been the stability of MOS gate. Typically, the threshold voltages Vth significantly shift after application of high positive and negative gate voltages over long period of time [5,6]. Fig. 2 shows typical degradation of the MOS gate in older devices without processing and structural improvements. As seen in these figures, high positive bias causes the Vth shift to positive side, while high negative bias does to negative side. Under the

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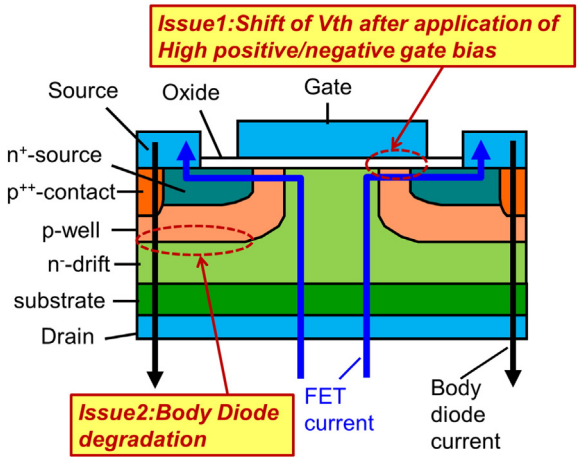

Fig. 1. Schematic cross-section of conventional SiC-MOSFET and its reliability issues.

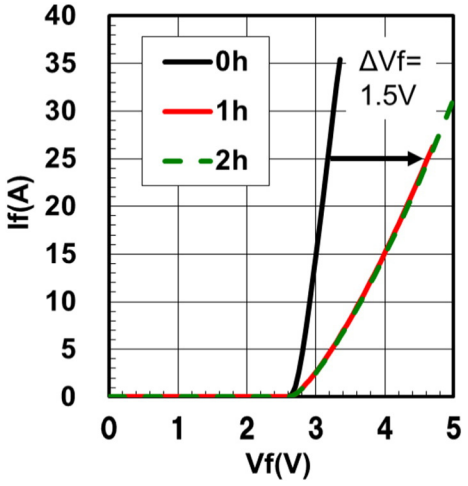

Fig. 3. Typical forward current–voltage characteristics of pn-junction-based body diode in a conventional SiC MOSFET after applying forward current of 15 A.

definition of Vth as the gate voltage giving the drain current of 1 mA at Vds = 10 V for the device with the rating current of 25 A, the shift of Vth with positive gate bias of +20 V is 0.6 V. The negative shift of Vth with high negative bias of −10 V is 1.5 V, which indicates that the value of the negative shift is more serious than that by positive bias. The negative shift would cause the change of the operation mode of the MOSFET from normally-off to normally-on and thus it is very serious for practical applications. Note that, as a mechanism of the above-mentioned Vth shift, it has been proposed that charge trapping or de-trapping at the interfacial states around SiO_2/SiC and also at traps in SiO_2. It has been reported that post-oxidation annealing passivates the traps and improves the Vth shift. Some reports mention that the Vth shift has been solved; however, these are still fully dependent on the detailed processing and device structure that is in general considered as know-hows.

In addition to the Vth shift, degradation of pn-junction-based body diodes in SiC MOSFET has been a serious reliability issue [7]. So far, significant increase of the forward voltage Vf of the pn-junction after applying forward bias has been observed as shown in Fig. 3.

The degradation of pn-junction in SiC MOSFET is believed to be caused by the expansion of basal plane dislocations (BPDs) in the SiC resulting in stacking faults of the crystal. Various methodologies to solve the issue by the improvement of SiC crystal growth have been demonstrated so far. These include the reduction of the BPD density itself [8] and converting the BPDs into threading edge dislocations (TEDs) during the epitaxial growth [9]. Connecting an external Schottky barrier diode (SBD) with smaller forward built-in voltage between the source and drain of the SiC MOSFET to avoid the current flow over the body diode has been a viable solution, since the reduction of the forward voltage for the reverse current is also critical to reduce the switching loss in the practical circuit. The use of SBDs is a good solution; however, it sacrifices the total chip area of the SiC resulting in higher cost and larger device size.

3. Structure and performances of diode-integrated SiC-MOSFET (DioMOS)

Here, a new structure of a SiC MOSFET called as DioMOS is described. The DioMOS has an extra channel layer underneath the gate oxide that serves a current path for the reverse conduction. This prevents the current from flowing onto the pn-junction-based and thus solves the reliability issue. The DioMOS can also serve the low built-in voltage diode for the reverse conduction by optimization of the channel design. Thus the DioMOS can eliminate the conventional SiC SBD to flow the reverse current as shown in Fig. 4. The elimination of an external diode can reduce the consumption of the area of SiC resulting in lower cost and smaller size of the packaging. Note that the elimination of the wiring between the SiC transistor and the SBD potentially enables smaller switching loss by the elimination of parasitic inductances. The following are the basic operating principle of the newly proposed DioMOS.

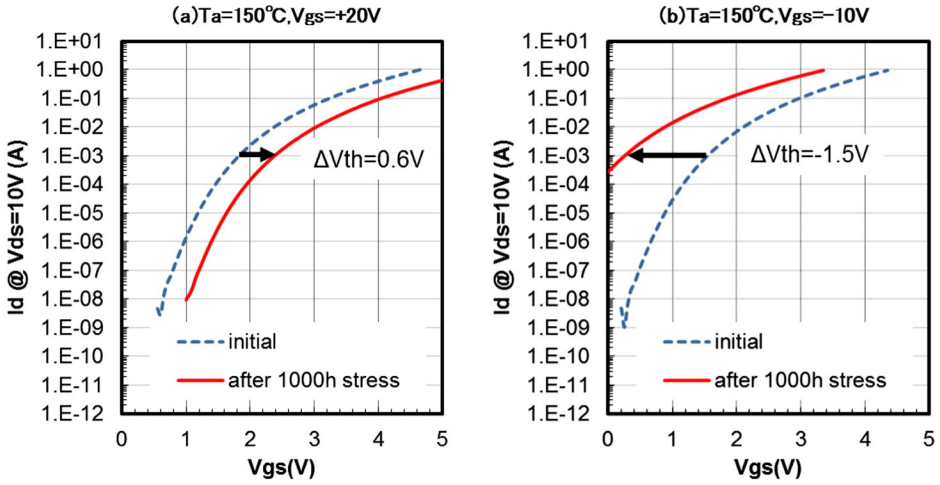

Fig. 2. Typical data of Vth shift after the application of (a) positive bias stress Vgs = +20 V, (b) negative bias stress Vgs = −10 V over 1000 h at 150 °C.

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