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Invited paper

SiC power MOSFETs performance, robustness and technology maturity

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ABSTRACT

Relatively recently, SiC power MOSFETs have transitioned from being a research exercise to becoming an industrial reality. The potential benefits that can be drawn from this technology in the electrical energy conversion domain have been amply discussed and partly demonstrated. Before their widespread use in the field, the transistors need to be thoroughly investigated and later validated for robustness and longer term stability and reliability. This paper proposes a review of commercial SiC power MOSFETs state-of-the-art characteristics and discusses trends and needs for further technology improvements, as well as device design and engineering advancements to meet the increasing demands of power electronics.

List of symbols

d	device thickness [cm]
$D_{n,p}$	diffusion coefficients [cm_2 s^{-1}]
$\vec{E}$	electric field [V cm^{-1}]
Ec	critical electric field value [V cm^{-1}]
E_g	energy bandgap [eV]
H	heat dissipation rate [W cm^{-3}]
$\vec{J}$	current density [$\frac{A}{cm^2}$]
J_{LEAK}	leakage current amplitude [A cm^{-2}]
n,p	electron, hole density [cm^{-3}]
n_i	intrinsic carrier concentration [cm^{-3}]
P_D	power density [W cm^{-3}]
q	electronic charge [C]
R_S	specific resistance [Ω]
R_θ	thermal resistance [K W^{-1}]
V	electrostatic potential [V]
V_{BR}	breakdown voltage [V]
V_{DS}	drain-source voltage [V]
V_{GS}	gate-source voltage [V]
T_{CASE}	case temperature [°C]
α_T	current temperature coefficient [A K^{-1}]
ε_r	relative dielectric constant [−]
λ_θ	thermal conductivity [W cm − 1 K^{-1}]
$\mu_{n,p}$	electron, hole mobility [cm^2 V^{-1} s^{-1}]
Z_θ	thermal impedance [K W^{-1}]

1. Solid-state devices in power electronics

Switches used in electrical energy conversion are primarily expected to enable transfer of energy between a source and a load, allowing for conversion of the electrical characteristics (e.g., voltage and current levels), with minimum energy losses in the process. Ideally, one would want devices featuring infinite current conduction capability with zero on-state voltage (i.e., conductor-like behaviour), infinite blocking voltage capability with zero off-state current flow (i.e., isolator-like behaviour) and instantaneous non-dissipative transitions between the on and off states. Semiconductor components enable approximating these behavioural features to a reasonable extent and with a considerable degree of design flexibility. However, in practice, the design of solid-state devices is necessarily characterised by trade-offs between on-state, switching and blocking performance. How closely a power device approximates an ideal switch is a very important figure of merit, key in the competition among manufacturers: indeed, the ability to conjunctly improve the above mentioned characteristics yields not only better efficiency and reduced stresses, but also, and probably more importantly, it enables to significantly decrease the size and weight of power converters by reducing electro-magnetic filters and heat-sink sizes, which is of paramount strategic value in a broad range of application domains.

1.1. Design for nominal function

Eq. (1) is most commonly used to describe the on-state behaviour of a semiconductor device (see [1–3], for example). A more detailed

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description also accounts for current components associated with temperature gradients (*Seebeck* effect) [4], but it is beyond scope in this context.

$$\vec{J} = q\mu_n n \cdot \vec{\nabla}V + qD_n \cdot \vec{\nabla}n + q\mu_p p \cdot \vec{\nabla}V - qD_p \cdot \vec{\nabla}p \quad (1)$$

The on-state current is the sum of drift and diffusion components, due to flow of both electron and holes, driven by gradients within the semiconductor crystal of the electro-static potential and the charge-carriers' density, respectively. More typically, devices are designed to make primarily use of drift current components of one charge carrier type and diffusion of the other type. So, for simplicity, in the following, reference is made to electron (n) drift currents and hole (p) diffusion currents. In a first approximation [4], the density of power dissipated during the on-state conduction (i.e., the heat generation rate) can be described as

$$\vec{J} \cdot \vec{E} = H = P_D \quad (2)$$

and is thus essentially related to the drift current components, the factors multiplying the voltage gradient in Eq. (1) being equivalent to a specific electrical resistance

$$\frac{1}{q\mu_n n} \cdot d = R_S. \quad (3)$$

So, to optimise on-state performance, relatively high doping levels and relatively large diffusion current components are desirable, with as thin as possible devices.

However, for a given material, the maximum doping level is typically dictated by the concurrent requirement for voltage withstand capability, the device breakdown voltage being inversely proportional to the carriers' concentration as

$$V_{BD} \propto \frac{\varepsilon_r}{2qn} \cdot E_C. \quad (4)$$

Minimum crystal thickness is in general limited by the need to contain the depletion region extension, which increases with blocking voltage capability as

$$W_D \propto \sqrt{\frac{2\varepsilon_r}{qn} V_{BD}}. \quad (5)$$

Also, the leakage current in a power device increases with both reverse bias voltage and intrinsic carrier concentration, the latter being a function of both temperature and energy band-gap [2,3], as

$$J_{LEAK} \propto \sqrt{V_{RB}} \cdot n_i. \quad (6)$$

Finally, diffusion currents require charge accumulation within the semiconductor crystal, which typically impairs the device switching performance.

1.2. Temperature considerations

Power devices operation is intrinsically characterised by heat generation and self-heating phenomena (see Eq. (2)). In the steady-state, the resulting change in device operational temperature is related to the power dissipation by

$$\Delta T = P_D \cdot R_\theta \quad (7)$$

with

$$R_\theta \propto \frac{1}{\lambda_\theta} \cdot d. \quad (8)$$

Temperature plays a major role in a number of considerations related to both the design and the theoretical performance of the devices [1–3,5]. Indeed, the design features of a semiconductor device are conditional to its doping levels always being much higher than the intrinsic carrier concentration: when this condition is no longer met, the device loses its intended characteristics. This poses a clear limit to the device maximum operational temperature capability. Over the allowed range, the actual temperature value affects on-state (e.g., decrease of carriers' mobility), off-state (e.g., increase of leakage current) and switching performance. Finally, the value of ΔT is central in determining the device reliability and operational lifetime.

1.3. SiC versus Si

Table 1 summarises the values of four selected material properties for Si and SiC. The critical electrical field of SiC is about seven times higher than that of Si. In view of the preceding discussion, it is clear how this characteristic alone has the important implication of enabling a significant increase of the doping level for a given target blocking voltage capability. This, in turn, leads straightforward to a reduction of the required minimum nominal thickness for a given voltage blocking capability. The result is that SiC devices can theoretically be designed with greatly improved on-state performance than their Si counterparts, or, conversely, devices with much smaller cross-section and higher blocking voltage than Si can be realistically designed, still with suitable on-state performance: this, notwithstanding a lower value of the carriers' mobility in SiC as compared with Si [3]. A reduction of the die cross-section goes in favour of switching performance, as it reduces the built-in capacitance. Also, with high enough doping and reduced thickness, reliance on large diffusion currents to achieve satisfactory on-state performance is less of a need and charge storage effects can be significantly reduced, with great advantages from a switching performance point of view.

Still after the values listed in Table 1, the intrinsic carrier concentration in SiC is about 20 orders of magnitude lower than in Si at room temperature. This has the twofold consequence of enabling the design of devices able to operate at temperatures well in excess of the typical maximum values found in Si, as well as designing devices with much higher voltage withstand capability than in Si for a given target performance. A nearly three-fold value of energy band-gap of SiC as compared to Si contributes to the design of devices with high temperature capability, thermally stable characteristics and intrinsically robust against a number of overload conditions. For reference, the energy bandgap in Si reduces from nearly 1.1 eV at 300 K to nearly 0.9 eV at 1000 K, whereas the change is from about 3.26 eV at 300 K to 3 eV at 1000 K for SiC [3].

Finally, the higher thermal conductivity value enables a reduction of the thermal resistance of the semiconductor die, which, in principle, can be taken advantage of by increasing the achievable power density for a given ΔT (i.e., device size for given current rating, see Eq. (7)) or by reducing ΔT for a given power density value. To which extent the reduced R_θ value of the die can be taken advantage of clearly depends on its relative importance in the overall thermal resistance value of the packaged device.

Table 1
Selected material properties of Si and SiC.

	E_C [MV/cm]	n_i (300 K) [cm^{-3}]	Eg [eV]	λ_θ [W/cm K]
Si	0.3	$1.45 \cdot 10^{10}$	1.12	1.5
SiC	2.0	$8.2 \cdot 10^{-9}$	3.26	4.5

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