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Formation mechanism of concave by dielectric breakdown on silicon carbide metal-oxide-semiconductor capacitor

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ABSTRACT

Adjacent concaves are formed commonly on silicon carbide (SiC) MOS capacitor after time-dependent dielectric breakdown (TDDB). This paper describes the formation mechanism of the concave on the SiC MOS capacitor with aluminum gate electrode on thermally grown silicon dioxide gate dielectric by the dielectric breakdown. At the bottom of an approximately 450 nm-deep concave, a stack structure of the concave surface was found to be surface oxide/C-rich layer/Si-rich layer/SiC substrate. Some C-rich debris adhered on the surface of the concave. The concave surface was speculated to be formed by a sequence of the C-rich surface on the Si-rich surface, the debris adhered on the surface, and the oxide layer containing nitrogen and aluminum. Formation of the concave and its surface is explained based on the physical properties of SiC; (i) a peritectic decomposition of SiC to the solid phase carbon and the liquid phase solution containing silicon and carbon, (ii) a normal freezing process of the liquid phase solution, and (iii) a thermal decomposition on the concave surface to form a graphite layer.

1. Introduction

Silicon carbide (SiC) attracts much attention as a material for a next-generation power electronics device thanks to its wide bandgap properties [1,2]. An advantage of SiC over other wide bandgap materials is that silicon dioxide film grows on SiC with a conventional thermal oxidation process for silicon [3]. However, reliability of the thermally grown oxide formed on SiC has been of great concern because of the residual carbon in the thermally grown oxide [4,5] and dislocations on the SiC substrate [6–8]. Although the degradation mechanism has been extensively investigated, few reports mentioned the reliability physics of the breakdown process of the SiC MOS structure; the relationship between the position of the dislocation and the dielectric breakdown revealed by the KOH-etching of the SiC surface [6,9].

A microscopic analytical study of the silicon CMOS device after the breakdown revealed breakdown processes. For instance, “self-healing” [10–12], i.e. the disappearance of the gate electrode by the joule heat generated by the dielectric breakdown. The device subjected to the self-healing behaves as a flesh device. Another example is “dielectric breakdown induced epitaxy” [13,14], i.e. the epitaxial growth of silicon toward the gate dielectric at the dielectric breakdown. These findings by the physical analysis successfully explained the electrical characteristics at the breakdown of silicon CMOS devices [12–15].

In our reliability study of the SiC MOS capacitor, “carpet-bombing-like” concaves, i.e. adjacent concaves, have been found to be formed commonly after the dielectric breakdown [16]. These concaves were found on the SiC MOS capacitors with both the aluminum electrode and the poly-silicon gate electrode as shown in Fig. 1(a) and (b), respectively. These results suggest that “carpet-bombing-like” concaves are commonly formed after the dielectric breakdown of SiC MOS capacitors, slightly depending on the gate electrode material.

Although these successive concaves are formed during the electrical breakdown, it is speculated that each concave is not a final breakdown path due to the “self-healing”. In our recent study, especially with respect to the SiC MOS capacitor with the aluminum electrode, the post-breakdown conduction path was found to be formed on the edge of the domain where the concaves were formed and aluminum electrode evaporated [17]. Therefore, the “carpet-bombing-like” concaves were considered to be formed during the intermediate breakdown process in a series of the breakdown events. This intermediate concave formation process has not been clarified yet. By a detailed analysis, it will be clarified that how this concave is formed. In this paper, a formation mechanism of the concave after the dielectric breakdown is investigated.

2. Experimental

A SiC MOS capacitor with a 237 nm-thick aluminum gate electrode on a 40 nm-thick thermally grown oxide was fabricated on a n-type

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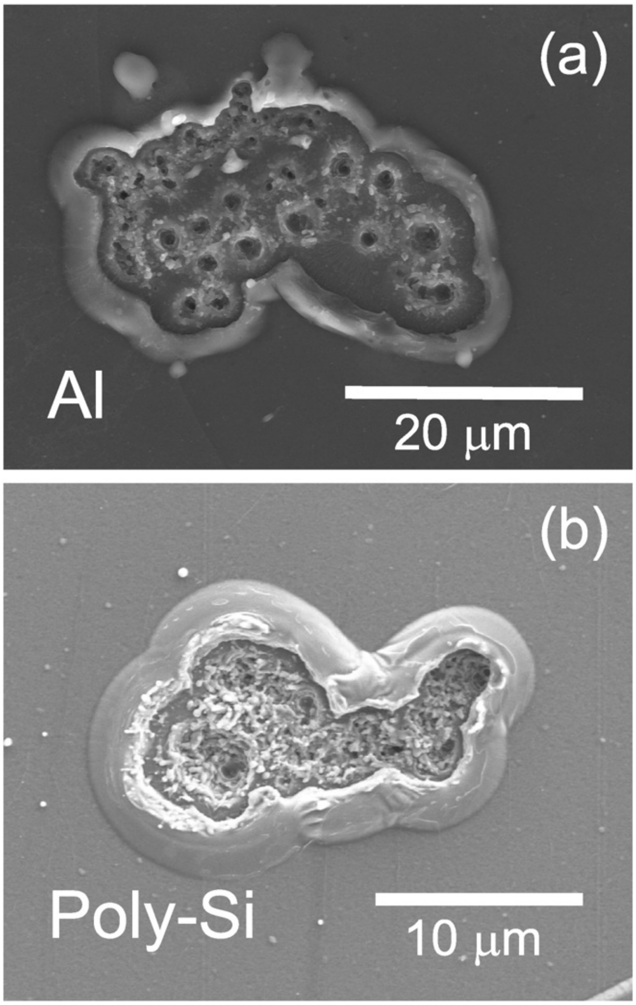

Fig. 1. (a) A scanning electron micrograph of the surface of the SiC MOS capacitor with aluminum (300 nm) electrode after the time-dependent dielectric breakdown. (b) A scanning electron micrograph of the surface of the SiC MOS capacitor with poly-silicon (400 nm)-on-aluminum (300 nm) gate electrode stack structure.

10 μm-thick epitaxial layer on a 4H-SiC wafer with 4° off-axis (0001) surface. A diameter of the circular device area was 150 μm. A TDDB testing was performed under a constant current stress of 200 nA with a positive gate bias voltage using an Agilent B1505A semiconductor parameter analyzer. After the TDDB measurements, the surface of the MOS capacitor was analyzed using a field-emission scanning electron microscope (FE-SEM) from JEOL (JSM-7800F) with an energy dispersive X-ray spectrometer (EDS). It should be noted that the sample was tilted during EDS analysis to avoid a shadowing in the concave. A transmission electron microscope (TEM) from JEOL (JEM-2100F) was employed to investigate the nano-structure of the concave surface. An electron beam incident direction was [1–100] of 4H-SiC substrate. For TEM–EDS measurement, the Cliff-Lorimer factor (*k*-factor) was adjusted to $k_{Si/C} = 3.695$ to obtain a composition ratio of Si:C = 1:1 at the SiC substrate. A specimen for a TEM analysis was prepared by means of a high energy gallium focused ion beam (FIB). A carbon film was deposited on the sample to protect the surface before the FIB sample preparation.

3. Results

A typical hard breakdown characteristic was observed during the constant current stress TDDB measurement of the SiC MOS capacitor as shown in Fig. 2. The gate voltage just before the breakdown (V_1) was 45.0 V, and the gate voltage just after the breakdown (V_2) was 0.331 V. After the breakdown, it was confirmed, by the FE-SEM, that “carpet-bombing-like” concaves were formed on the surface of the MOS capacitor. It should be noted that the “carpet-bombing-like” concaves are found to be formed commonly through our experiments.

A SEM image and corresponding element distribution images of the concave surface of the measured MOS capacitor by means of SEM–EDS analysis are shown in Fig. 3(a)–(e). Almost all of aluminum electrode was found to evaporate around the concaves. As shown in Fig. 3(c), at the bottom of the concave, a Si-rich surface was found to be formed. SEM–EDS peak signal intensities of C K_α, O K_α, Al K_α, and Si K_α spectra at each point in Fig. 3(a) are summarized in Table 1, which indicates the Si-rich surface at the bottom of the concave (point 1 in Fig. 3(a)) compared to the surface around the concave. This finding is also confirmed at other concaves formed by the dielectric breakdown.

A nano-structure of the concave surface is investigated in detail by means of cross-sectional TEM (XTEM). Fig. 4(a) shows a bright field XTEM image of the concave along a dashed line in Fig. 3(a). The diameter and the depth of the concave are approximately 950 nm and 450 nm, respectively. It should be noted that some defect-like areas were formed near the surface of the concave as indicated by the dashed moving border in Fig. 4(a). Three characteristic regions were found in a high-angle annular dark filed scanning TEM (HAADF-STEM) image in Fig. 4(b). In the region 1, a typical surface on the concave was found. In the region 2, a large debris was found on the surface of the concave. In the region 3, a more severe defect-like region than those in regions 1 and 2 was found in the SiC substrate around the bottom of the concave.

For the analysis of the region 1, a line scan TEM–EDS analysis was performed along a line with dots in a HAADF-STEM image in Fig. 5(a) and its result is shown in Fig. 5(b). This result indicates that an approximately 2 nm-thick C-rich layer was formed on the approximately 20 nm-thick Si-rich layer, schematically illustrated above in Fig. 5(b). In addition, it is worth noting that the Si-rich layer appears darker compared to SiC substrate in a HAADF-STEM image in Fig. 5(a). This result indicates that the density in the Si-rich layer is much low than the SiC substrate since the contrast in a HAADF-STEM image is generally affected by a square of an atomic number and a density. It was found that the oxide film that contains nitrogen and aluminum was formed on the thin C-rich layer. Since nitrogen and aluminum were not incorporated in the

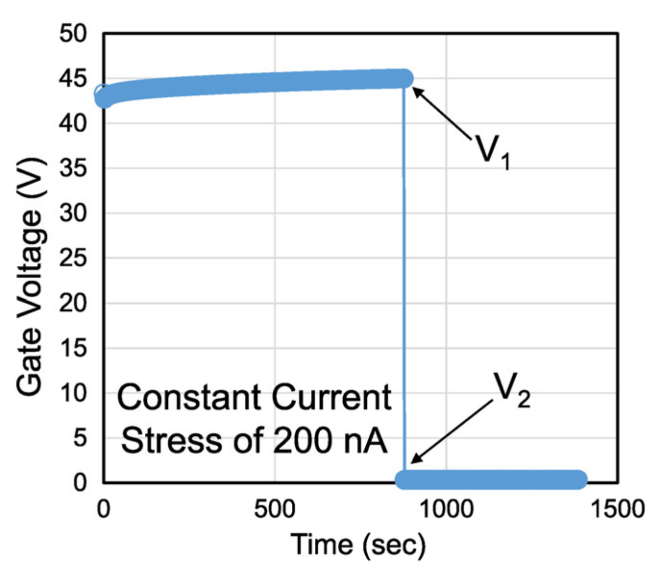

Fig. 2. A time-voltage characteristic obtained by time-dependent dielectric breakdown (TDDB) measurement of a SiC MOS capacitor under a constant current stress of 200 nA with positive gate bias voltage. The gate voltage just before and after the breakdown are indicated by V_1 and V_2, respectively.