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A distributed minority and majority voting based redundancy scheme

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ABSTRACT

This article presents a new distributed minority-cum-majority voting based redundancy (DMMR) scheme that is scalable and has the ability to tolerate multiple function module faults/failures. In comparison with 5-tuple, 7-tuple, and 9-tuple versions of the N-modular redundancy scheme, the proposed DMMR scheme whilst being equally fault-tolerant reports respective improvements in design metrics (i.e., figure-of-merit) by 32.5%, 180.4% and 377.4% for example ASIC-based implementations utilizing a 4×4 array multiplier as the representative function module, whilst reporting very small corresponding decreases in system reliability by just 1.21%, 1.06% and 1.08% for consideration of module reliabilities ranging from 0.9 to 0.99. The simulation results are obtained using a 32/28 nm CMOS process.

1. Introduction

Mission and safety-critical applications, by default, employ redundancy in system design to overcome any arbitrary function module fault(s)/failure(s) to provide correct and uninterrupted operation [1]. The function module deployed could be any circuit/system that is duplicated as per need to construct a redundant system. In a passive N-modular redundant system, $(N-1)$ copies of a function module are used, and at least a majority M out of the N function modules is required to operate correctly to guarantee the mission-success [2,3]. In other words, the fault-tolerant N-modular redundant system is capable of accommodating maximum of $(N-M)$ function module failures. All the N function modules are joined using a voting element and the voter produces a majority vote based on the correct operation of M out of N function modules.

Triple modular redundancy (TMR), which is a 3-tuple version of the generic NMR, deploys 3 function modules and at least any 2 of the 3 function modules are expected to operate correctly, i.e., the TMR can cope with only 1 function module fault/failure. To cope with scenarios where multiple function module faults or failures are likely to occur, such as the possibility of multiple fault occurrences in combinational and/or sequential systems due to radiation phenomena [4,5], higher versions of the NMR such as 5MR (which is a 5-tuple version of NMR), 7MR (which is a 7-tuple version of NMR), or even 9MR (which is a 9-tuple version of NMR) may be used selectively [6]. However, the main drawback of higher order NMR systems such as 5MR, 7MR and 9MR is the exacerbated increase in design metrics viz. power, delay, and area. To mitigate the large design overheads of higher order redundant systems, this paper proposes a new distributed minority and majority voting based redundancy scheme, called the DMMR. The DMMR is scalable and is found to be efficient in terms of design parameters for comparisons of sample ASIC-based implementations of 5MR, 7MR and 9MR designs with counterpart DMMR designs.

In the rest of this paper, Section 2 describes the conventional NMR and proposed DMMR system architectures through block schematics. The system reliability equations of 5MR, 7MR, 9MR, and the proposed 3-of-5, 3-of-6 and 3-of-7 DMMR systems are given in Section 3. The system reliability curves of various systems are plotted as a function of their module reliabilities. Section 4 presents the simulation results obtained for sample implementations of 5MR, 7MR, 9MR, 3-of-5 DMMR, 3-of-6 DMMR and 3-of-7 DMMR systems by considering a 4×4 array multiplier as a representative function module. Lastly, Section 5 provides the conclusions.

2. Illustration of NMR and DMMR schemes

The generalized block schematics of NMR and DMMR schemes are portrayed by Fig. 1a and b respectively. In the NMR system, $(N-1)$ copies of a function module i.e., N identical function modules are used and the majority voter combines the outputs of the N function modules viz. M_1 to M_N to produce a majority vote (NV) indicating the correct NMR system operation. In order to satisfy the majority logic, at least $(N+1)/2$ out of the N function modules should maintain the correct operation, where N is odd.

In Fig. 1b, F_1 up to F_N represents the outputs of the function modules 1 to N. According to the proposed DMMR scheme, the function modules are split into two groups, which are highlighted as the portions enclosed

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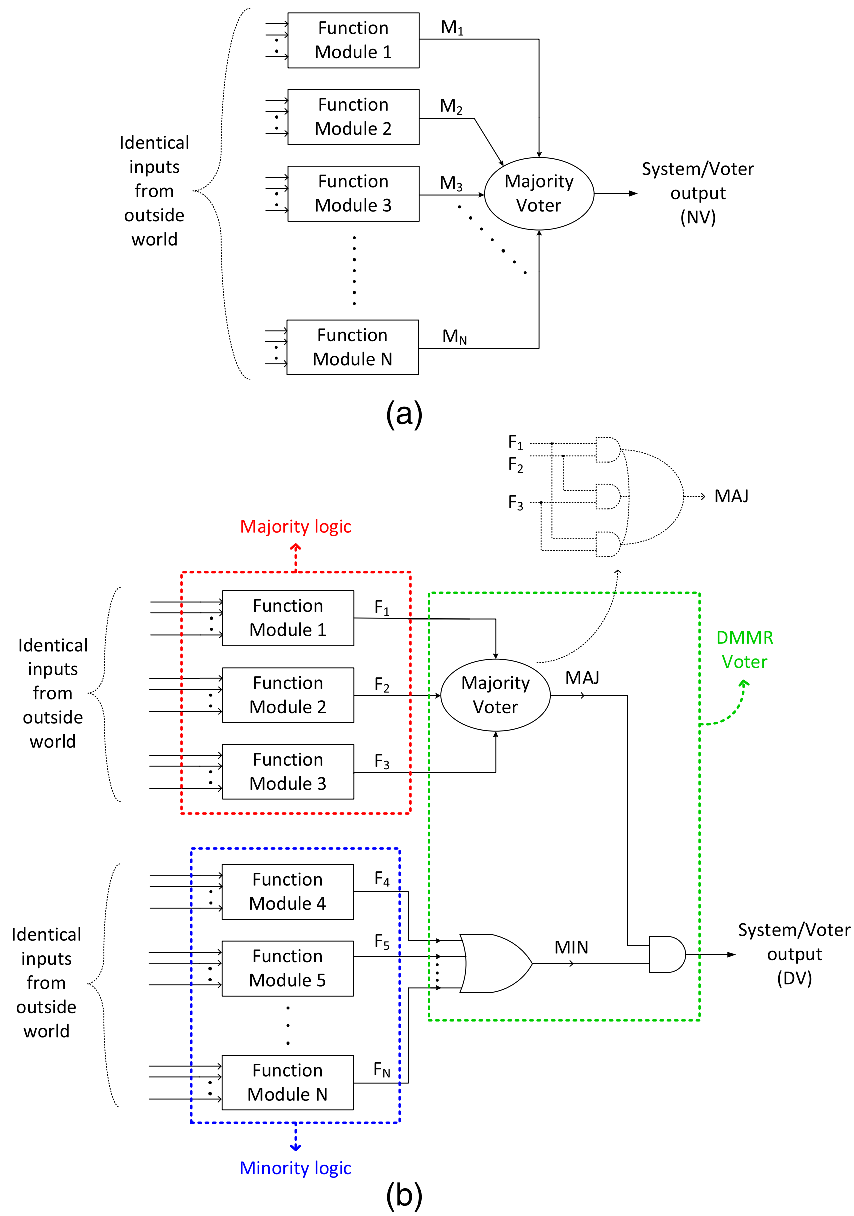

Fig. 1. Block diagram representation of (a) NMR, and (b) the proposed DMMR scheme. (For interpretation of the references to colour in this figure, the reader is referred to the web version of this article.)

within the red and blue dotted lines in Fig. 1b, named as *majority logic* and *minority logic* respectively. The outputs of function modules 1, 2 and 3 viz. F_1, F_2 and F_3 are fed to a 3-input majority voter, which implements the sum-of-products $F_1F_2 + F_2F_3 + F_1F_3$ using a single complex gate viz. the AO222 cell, shown using dotted lines in Fig. 1b. Function modules 4 to N (where N is a positive integer, and $N > 3$) are considered separately and their outputs are fed to an OR gate, which implements the logical disjunction: $F_4 + F_5 + \ldots + F_N$. The *majority logic* requires that any 2 out of the 3 function modules should operate correctly, i.e., the failure of any one arbitrary function module is alone tolerated. The *minority logic* requires at least 1 arbitrary function module to maintain the correct operation. In a DMMR system, as a minimum, 4 function modules are used with 3 function modules constituting the majority logic, and the remaining function modules constituting the minority logic. When N function modules are employed in a generic 3-of-N DMMR system, 3 function modules would comprise the majority logic and the remainder of the function modules viz. $(N - 3)$ would comprise the minority logic. The respective outputs of the two logic groups of function modules (i.e., majority logic and minority logic) viz. MAJ and MIN are combined using a 2-input AND gate that produces the system/voter output (DV), as indicated in Fig. 1b.

The DMMR voter, shown within the green dotted rectangle in Fig. 1b, is not only fault-tolerant but also incorporates inherent error correction capability. To explain these, let us consider two example scenarios for illustration with reference to Fig. 1b.

Let us presume that the expected (correct) values of F_1 up to F_N are 1, subject to the application of specific inputs. Under this scenario, MIN and MAJ would equate to 1, and the correct voter output $DV = MAJ \cdot MIN = 1$. Supposing multiple function modules become faulty or fail, for example, assuming that function module 1, and function modules 5 up to N become faulty/fail and as a result their outputs get corrupted, F_1, and F_5 up to F_N would become 0 instead of 1, whilst function modules 2, 3 and 4 would alone retain the correct value of 1. Still the internal voter outputs MAJ and MIN would