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Effect of source and drain asymmetry on hot carrier degradation in vertical nanowire MOSFETs

Jae Hoon Lee [a], Jin-Woo Han [b], Chong Gun Yu [a], Jong Tae Park [a,*]

[a] Department of Electronics Engineering, Incheon National University, #119 Academi-Ro Yoonsu-Gu, Incheon 406-772, South Korea
[b] NASA Ames Research Center, Moffett Field, CA 94035, USA

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ABSTRACT

Effects of source and drain (S/D) asymmetry on hot carrier degradation in vertical nanowire MOSFETs have been investigated with different nanowire radiuses. The S/D asymmetry causes different degree of hot carrier degradations between forward and reverse stresses. The actual stress voltage applied to the channel as a result of parasitic resistance and gate to junction overlap length is attributed to the cause of the asymmetric degradation. The narrower nanowire also suffers from worse hot carrier effects due to current crowding and geometric effects.

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1. Introduction

Due to the excellent short channel effect immunity and the improved device performances, silicon nanowire MOSFET is generally considered as one of the most promising candidates for next generation CMOS technology [1–3]. There are two nanowire devices based on nanowire orientation: namely, lateral type and vertical or pillar type. As well known, a vertical MOSFET isolates the pillar body from the substrate and has much smaller footprint than the lateral one [4,5]. Since the vertical MOSFETs have advantages of occupying lowest silicon area and high device density, recently they have received with considerable attention for application of nonvolatile memory and stacked surrounding gate memory [6,7]. However, due to two different ion implantation to form a bottom source and a top drain region, a vertical MOSFET has different source and drain resistances (R_S and R_D), which results in the asymmetric characteristics. The device performances and reliability including, drive current, transconductance, cut-off frequency, and hot carrier degradation, depend on the source and drain resistance [8,9]. Therefore, it is of interest to investigate the effect of extrinsic asymmetry on hot carrier degradation in vertical MOSFETs. In previous work [10], the effects of graded channel doping profiles in vertical MOSFET and gate-drain/source overlap effects in asymmetric MOSFET on the hot carrier degradation have been reported. There has so far no experimental study to understand the effects of extrinsic asymmetry on hot carrier degradation in vertical MOSFETs.

In this work, we investigated the hot carrier degradation in the vertical nanowire MOSFET under forward and reverse stress conditions and with different nanowire radius (R_W).

2. Transistor details

Vertical nanowire MOSFETs fabricated on p-type bulk wafer were studied. Phosphorus (1 MeV/5E14 cm^{-2}) was implanted vertically at 7 tilt to form the source. Boron (120 KeV/8E13 cm^{-2}) was implanted for p-channel and arsenide (80 KeV/3E15 cm^{-2}) and phosphorus (50 KeV/5E14 cm^{-2}) were co-implanted vertically at 7 tilt to form the drain. Arsenide was introduced to form an abrupt junction near drain for increasing hot carrier injection in the flash memory. Since a high energy arsenide implant to the source causes damage into the crystal, phosphorus was implanted to form the source and a low energy arsenide implant was selectively conducted to form the drain. After activation of the dopants, Si etching was carried to form vertical pillars. The exposed Si pillars with a height of 450 nm were obtained after deposition and planarization of high density plasma SiO_2. Tunneling oxide of 5 nm, Si_3N_4 of 6 nm and blocking oxide of 8 nm were grown and deposited, sequentially. The metal of Ti/TiN/W (20/10/150 nm) was deposited for the gate electrode and patterned to form vertical MOSFET. Fig. 1(a) and (b) show a schematic view and doping concentration profile along the channel length of tested vertical MOSFET. A SEM image in Fig. 1(c) shows a conical shape of pillar in vertical MOSFET. The tested device shows asymmetric doping concentration profile in the source and drain and result, lead to the different R_S and R_D. Since there is no high energy/high current implant equipment, the maximum dose of the high energy equipment is limited by the tool itself. If the multiple

* Corresponding author.
E-mail address: jtpark@incheon.ac.kr (J.T. Park).

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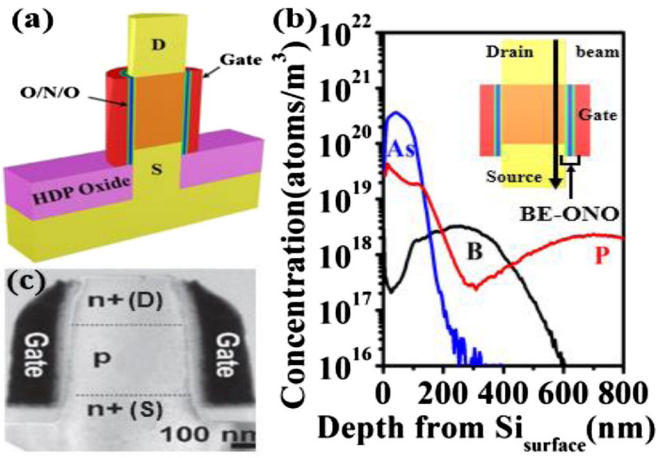

Fig. 1. Schematic view (a) and doping profile along the channel length (b) of tested vertical MOSFET.

implants are repeated to increase doping concentration of the source, the significant crystal damage is introduced. Therefore, asymmetrical doping concentration of source and drain for the vertical transistor is usual. The test devices also have the lightly doped drain extension and the Gaussian doping concentration profile in the channel region. The gate length was 250 nm and R_W ranged from 85 nm to 565 nm. In order to characterize hot carrier degradation, we used stress V_{DS} and stress V_{GS} -V_{TH} were 4.0 V and 4.0 V, respectively.

3. Results and discussion

The asymmetric characteristics of vertical MOSFET were observed from the measured transfer curve at $V_{DS} = 0.1$ V as shown in Fig. 2 by S/D swapping. The ON current in the forward measurement is larger than that in the reverse measurement at the same V_{GS}. In case of vertical MOSFET where R_S tends to be larger than R_D, ON-current in the reverse measurement is expected to be larger than that in the forward measurement due to the source side series resistance. However, the contradictory result is observed. The first reason is the high injection of electrons from the source to the channel in the forward measurement. Since the doping concentration of the source is lower than that of the drain, the potential barrier in forward is lower than that in reverse. As result, the electrons can easily be injected from the source into the channel region. The

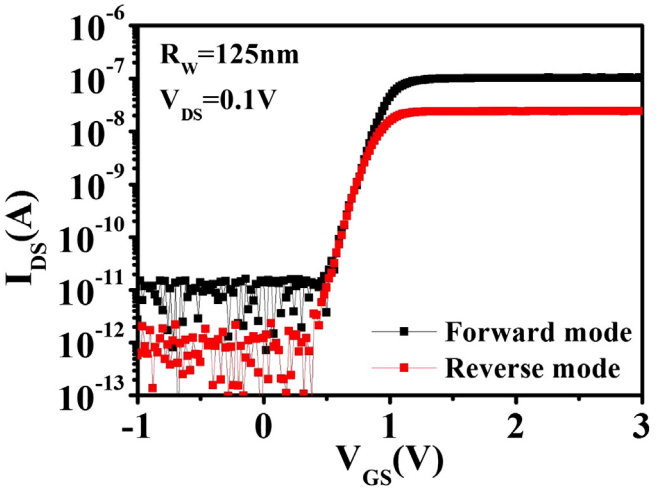

Fig. 2. A plot of the transfer curves of $R_W = 125$ nm in the forward and the reverse measurements.

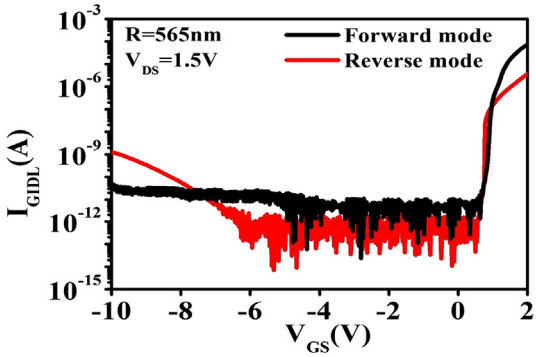

Fig. 3. GIDL current characteristics of $R_W = 565$ nm in the forward and the reverse measurement.

larger OFF leakage current in the forward measurement than that in the reverse measurement supports the higher thermionic injection due to the low potential barrier. The second reason is less-overlap region formed between the gate and the drain due to the gate recess below the drain junction. The less-overlap at the drain region is verified from that the larger GIDL (Gate Induced Drain Leakage) current in the reverse measurement than that in the forward measurement as shown in Fig. 3. The less-overlap at the drain region was not intentionally made, but it may be formed by the process. As the vertical gate length is not readily controlled, we did not pay much effort to align the junction and the edge of the gate. A conical shape of a pillar inherited from the process may be the third reason for the increased ON current in the forward measurement.

In order to investigate the asymmetry of the source and the drain on hot carrier degradation, the measured output characteristics under forward and reverse stress conditions were shown in Fig. 4. The devices were stressed at $V_{DS} = 4.0$ V and V_{GS} -$V_{TH} = 4.0$ V for 60 min. The device degradation is more severe in forward stress than in reverse stress. The reasons will be discussed in the last section.

Fig. 5 shows a plot of hot carrier induced drain current degradation in saturation region ($\Delta I_{DS}/I_{DS}$) as a function of R_W under forward and reverse stress. The devices were stressed at $V_{DS} = 4.0$ V and V_{GS} -$V_{TH} = 4.0$ V for 60 min. It is worth to noting that the device degradation under both forward and reverse stress conditions is increased as R_W decreases. According to the previous report [11,12], hot carrier degradation in multiple gate MOSFETs has been shown either decrease or increase with decreasing fin width. It has also been reported that hot carrier degradation has been increased for narrow diameter devices in gate all around twin silicon nanowire field effect transistor due to the increased vertical electric field at nanowire surface [13].

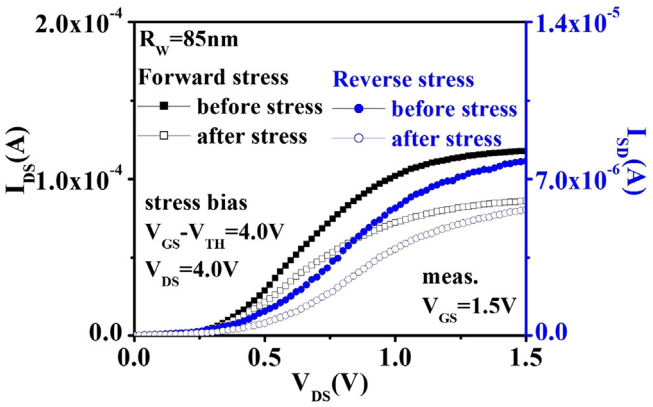

Fig. 4. Output characteristics before and after forward and the reverse stress.

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