Microelectronics Reliability 55 (2015) 1574–1578

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Failure analysis on recovering low resistive via in mixed-mode device

M. Castignolles *, J. Goxe, R. Martin

Freescale Semiconducteurs France SAS, Toulouse Product Analysis Laboratory, France

ARTICLE INFO

Article history:
Received 25 May 2015
Accepted 23 June 2015
Available online 5 August 2015

Keywords:
Failure analysis
OBIRCH
Resistive via
TEM
EFTEM
Recovery

ABSTRACT

In this paper, it will be presented the FA flow used to localize and characterize a recovering resistive via on die business customer rejects on an analog automotive integrated circuit with a mature technology. Despite the use of advanced FA techniques and tools, both electrical and physical analyses were challenging due to the recovery failure and to the difficulty to quantify the subtle variation at metal1/metal2 interface between a fail and a reference via. Finally, a comparison of different FA techniques applicable to our case to localize with success a recovering resistive via without modifying the initial failure will be discussed.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

In modern failure analysis (FA) in both digital and analog worlds, finding the locations of resistive defects, such as a resistive via, could be very challenging [1–3], and even more when the parts are recovering [4,5]. Various and complex tools and associated techniques are mandatory for the FA process to overcome the technical challenges.

The topic of this paper deals with the FA flow used to localize and characterize a recovering resistive via on die business customer rejects on an analog automotive integrated circuit with a technology above one micrometer.

In the Electrical failure analysis (EFA) section, it will be presented our approach to overcome the recovery of the parts in order to obtain a localization of the defective area. In the following section, it will be shown that physical failure analysis (PFA) can also be very challenging on technology above 1 μm. Having very complex and expensive FA tools are not always sufficient to determine the origin of the root cause. Finally, a discussion will be held on what are our solutions to detect with success a recovering resistive via.

2. Problem definition

Customer reported 14 defective components. All of them share the same failure signature: Vreg voltage output is higher than the specified value (+1 V). Customer noticed this issue when testing the parts at room temperature after assembly in the TO3 package. This assembly process requires a high temperature (above 400 °C) for the die attach process. Those customers' returned parts were the first quality excursion after the product fabrication was transferred to another factory.

3. Electrical failure analysis

3.1. Repackaging process and failure verification

Usual FA flow for die business product starts by unsoldering the silicon die from the customer package, and then it is repackaged in a ceramic DIL28 package in order to have access to more connections for advanced electrical characterization and for automatic test equipment (ATE) testing. After this repackaging process, the failure verification is performed. The first repackaged part did not exhibit the high Vreg issue and the part was fully functional. Failure recovery could be due to mechanical/thermal constraint during repackaging but could also be a consequence of bias/current influence of the functional testing. The next defective part to be analyzed was not repackaged in order to lower the recovery event risk.

3.2. Microprobing analysis

Vreg is directly linked to BandGap voltage so the first step of EFA was to verify this value thanks to micro-probing. It was found higher than normal. Thermal compensation (TC) value can be adjusted by fuse selection of various combinations of resistors to change the 'PTAT' component of the bandgap (Fig. 1). The fuse state can be determined thanks to high magnification optical microscopy. Fuse states appeared to be correct. The next step was to verify this statement by measuring the resistance value. Micro-probing and I(V) characteristics were performed between the different TC pads (TC0, TC1, TC2 and TC3) and ground with a current-clamp at 100 μA. An abnormal high resistance was

* Corresponding author.
E-mail address: marie.castignolles@freescale.com (M. Castignolles).

http://dx.doi.org/10.1016/j.microrel.2015.06.149
0026-2714/© 2015 Elsevier Ltd. All rights reserved.

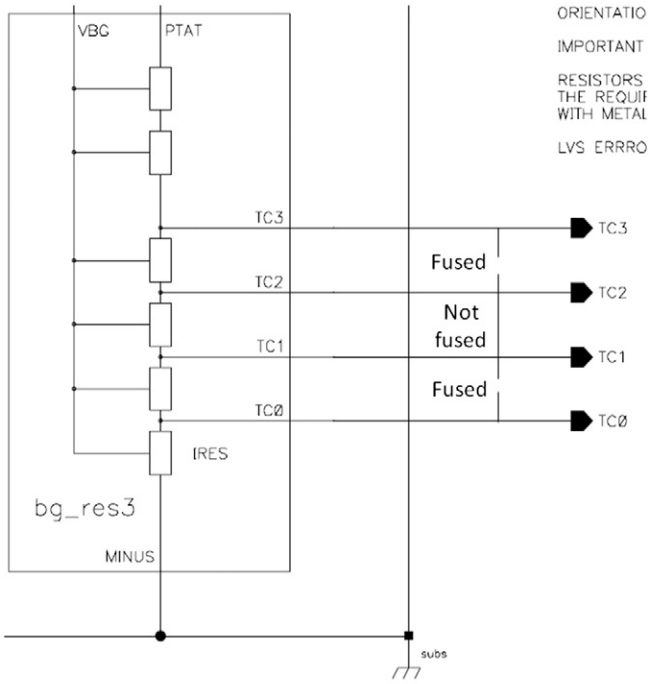

Fig. 1. Electrical schematic of the bandgap resistor bridge.

found between TC3 and ground (+2.5 kΩ). Further measurements showed that this extra resistance was located between TC3 and TC2. After those measurements, the failure recovered and Vreg were measured within specification. At this time, it was not known if mechanical constraint induced by TC pad micro-probing or current injection due to I(V) measurements was responsible of the recovery event.

Following failure analysis had to be done with special care regarding those constraints. First it was decided to use soft micro-probing needles to lower the mechanical constraint. Secondly, voltage measurements in functional mode were preferred as this approach was not injecting extra current through the resistive defect.

Another part was analyzed by taking into account the cares previously described (no repackaging, use of soft micro-probing needles and voltage measurement instead of I(V) for resistance measurement). One FIB test point was performed on the net connected to TC2 pad and voltages were measured in a functional mode. The results showed a voltage drop (104 mV) between the FIB test point and the TC2 pad, meaning the resistive defect is located between these two locations.

3.3. OBIRCh analysis

Thermal Laser Stimulation analysis was performed. The set up is the following: the component was not powered up (non-functional mode) and a voltage was applied between TC3 and ground. This voltage was chosen lower than the one measured on TC3 in functional mode in order to have a low current as it was suspected that high current could make the failure disappear.

Abnormal laser sensitivity was observed at a via1 location, indicating the resistive defect location close to TC2 pad (Fig. 2). During the OBIRCh analysis the part partially recovered: the value of the resistive defect decreased.

4. Physical failure analysis

4.1. Without any electrical localization

Due to cycle time, to the presence of several customer rejects, and to the fact that the parts were recovering, construction analysis was first performed in PFA. These analyses (FIB cross-sections on the contacts and vias, delayering, optical inspection of metal lines…) help us to discard a lot of branches in the fault tree analysis. In parallel, commonality analysis and wafer fabrication parameters were analyzed. Construction analysis and lot processing analysis were not able to pinpoint any process anomaly that could explain the origin of the increase of the resistance. As this technology is mature, several databases are available on this technology. No similarity could be found.

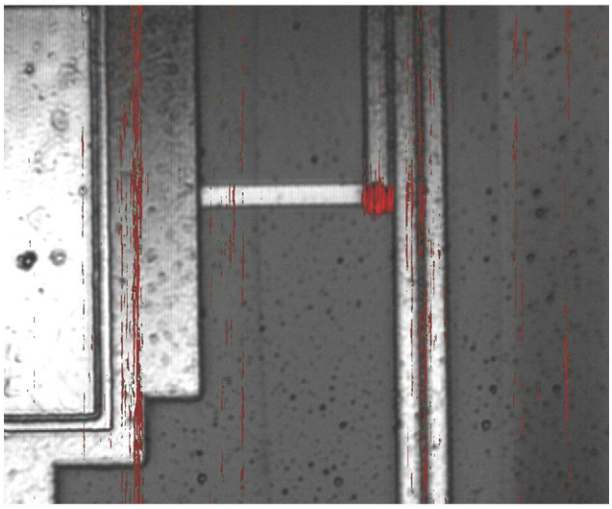

Fig. 2. OBIRCh image highlighting the defective via.

4.2. With a precise electrical localization

Finally, an electrical localization successfully highlighted a defective metal1/metal2 via on a customer reject. FIB cross-section was first performed on this via. FIB cross-section was not able to show any anomaly. Despite the size of the technology, a TEM cross-section was performed on this via. A TEM lamella is only 100–150 nm thick, in comparison with a metal1–metal2 via of this technology around ~3–4 μm large. TEM lamella evidenced the presence of an abnormal dark layer at metal1 aluminium/metal2 aluminium interface. On this technology metallization is aluminium with no Ti or TiN on the surface of the metal. This layer was suspected to be at the origin of the higher resistivity measured on this via. Another TEM cross-sections were performed on defective and reference vias. The same dark layer was observed on all the vias (Fig. 3). Higher magnification pictures evidenced two main differences: higher presence of voids detected in the dark layer (porous aspect) and interface layer seems slightly thicker on fail samples (Fig. 4). Energy filter TEM (EFTEM) [6,7] analysis detected the presence of oxygen (oxide layer) at metal1/metal2 interface on reference and fail via (Fig. 5). Therefore, the thickness of the oxidize layer seems thicker on the defective vias. No precise measurements of this layer could be performed. These results make very difficult to have a precise evaluation of what is a good or a fail via, and to optimize the manufacturing process.

Finally, a TEM cross-section was performed on die which was produced in previous factory. On this sample, the dark layer is present, but EFTEM and EDS analyses were not able to detect the presence of oxygen at metal1/metal2 interface.

This sample clearly demonstrated that the resistive issue is linked to this oxide layer at metal1/metal2 interface.

5. Failure mechanism & yield improvement

The failure analysis demonstrated the presence of a dark layer with the presence of oxygen at metal1/metal2 interface. This oxide only appears above 400 °C during the soldering on TO3 package at customer's

Download English Version:

https://daneshyari.com/en/article/6946653

Download Persian Version:

https://daneshyari.com/article/6946653

Daneshyari.com