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Electrical model of an inverter body-biased structure in triple-well technology under pulsed photoelectric laser stimulation

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ABSTRACT

This study is driven by the need to optimize reliability and failure analysis methodologies based on laser/silicon interactions with an integrated circuit using a triple-well process. Nowadays, single event effect (SEE) evaluations due to radiation impacts are critical in fault tolerance and security field. The prediction of a SEE occurring on electronic devices is proposed by the determination and modeling of the phenomena under pulsed laser stimulation. This paper presents measurements of the photoelectric currents induced by a pulsed-laser on an inverter in a triple-well Psubstrate/DeepNwell/Pwell structure dedicated to low power body biasing techniques. It reveals the possible activation change of the parasitic bipolar transistors. Based on these experimental measurements, an electrical model is proposed that makes it possible to simulate the effects induced by photoelectric laser stimulation. Therefore this electrical model could be used as a tool for characterizing more complex CMOS circuits under photoelectrical laser stimulation.

1. Introduction

Faults known as single event effects (SEEs) were first discovered in the 1960s when it was found that radioactive particles were causing errors in electronic circuits [1,2]. The aerospace industry directly affected by this issue began research on the physical effects of these particles in silicon. In this context, the use of pulsed-lasers was introduced to emulate SEEs at the experimenter's bench [3]. Today, a SEE is still a major threat for semiconductor manufacturers. Photoelectric laser stimulation (PLS) is commonly used in reliability evaluation and failure analysis methodologies [4]. However this kind of experiments can be very expensive and time consuming. In this context, it is interesting to use a simulation tool at the gate level in order to simulate with good accuracy the effect of PLS on a chip in order to analyze its impact in a very small amount of calculation time.

PLS generates electron–hole pairs in silicon, provided that the laser energy is greater than the silicon band gap. Our PLS experiments were carried out using a pulsed-laser at 1064 nm wavelength on the active parts of an inverter device in a triple-well structure (designed in 90 nm STMicroelectronics CMOS technology). PLS was performed through their backside, with a laser spot diameter of 1 μm and a laser shoot duration of 5 μs. This pulse duration range is more common in failure analysis and security than in a radiation field. For our measurements a wide range of laser pulse durations from short ns to long μs was used, nevertheless long pulse duration results were more relevant. The data we gathered were then used to design and calibrate an electrical model dedicated to PLS with a SPICE-like simulation. It makes it possible to simulate the response of an inverter in a triple-well structure to laser pulses. This is a first step toward simulation and understanding of PLS of more complex logic cells.

It has been shown [5] that inside the space charge region of a PN junction, electron–hole pairs will be separated by the internal electric field and then generate an optical beam induced current. The photoelectric currents created during the light stimulation flow through the PN junctions and may corrupt the cells' voltage output. In this paper, we also consider the parasitic bipolar junction transistors inherent to CMOS bulk devices. We show that these parasitic transistors contribute to the corruption of output cells at a higher rate than just the PN junctions of the OFF MOS side. Furthermore, in [6] an inverter under PLS for the case of a standard CMOS bulk process was already studied and modeled. The novelty of this paper is that our model, based on actual electrical measurements, takes into account the parasitic bipolar transistors topologically added by the use of a triple-well implant for the body-biasing techniques (see Fig. 1).

In triple-well, a Deep-Nwell implant (DeepNwell) is used to isolate the substrate of the NMOS transistors from the Psubstrate of the chip, hence creating Pwells as depicted in Fig. 1. The biasing of the DeepNwell is provided through the Nwell.

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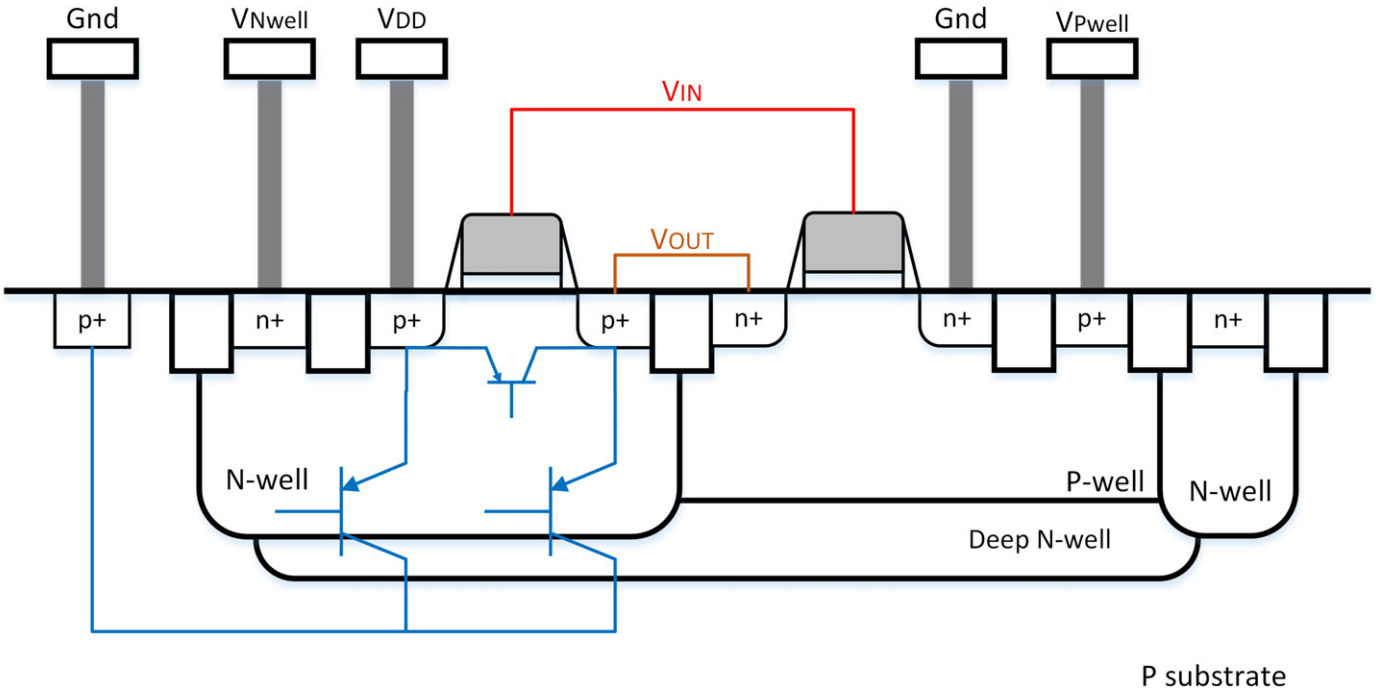

Fig. 1. Cross sectional view for an inverter in triple-well technology with parasitic bipolar transistors highlighted in blue.

With technology scaling down, performance and power consumption play an increasingly important role in logic design. The body-biasing technique presented in [7,8] is one well-known solution to optimize consumption and performance. This low-power technique uses threshold voltage scaling by reverse or forward body bias. In 90 nm CMOS technology with a power supply of $V_{DD} = 1.2$ V, the body biasing range is ± 400 mV applied on both NMOS and PMOS bulks (i.e., applied on the N and P wells), where the DeepNwell implant is needed. The first electrical models of MOS transistors under pulsed-laser stimulation were generally made of a current source which represents the photocurrent induced by the laser. In this paper we propose an improvement of these electrical models in order to take into account the triple-well implant.

This article first explains our models of the PN junctions under PLS as well as parasitic bipolar effects. Then, it shows the measurements of the inverter inside the triple-well when Input = Gnd and Input = V_{DD}. Finally, our electrical model and 3D simulation methods are proposed.

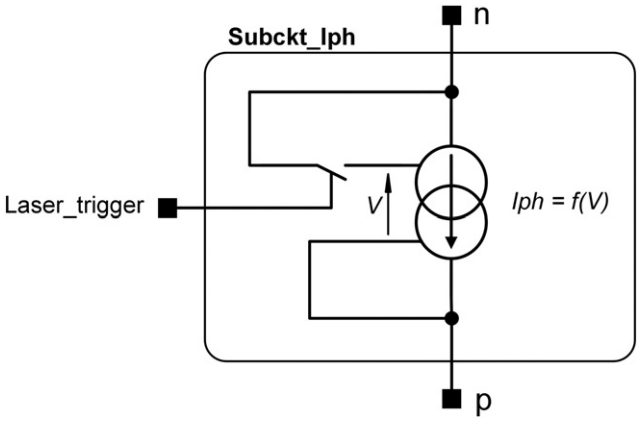

Fig. 2. Electrical modeling of a PN junction under pulsed laser embedded in a sub-circuit called Subck_Iph.

2. Photocurrent electrical model

Photocurrents generated by a pulsed-laser on an integrated circuit were generally modeled by current sources on PN junctions. We chose to improve the electrical model already introduced by Sarafianos et al. in [9,10], which takes into account the laser's spot size, power, pulse duration and focus of the laser beam as well as the spatial parameters, location, geometry and wafer thickness.

2.1. PN junction modeling

Using a laser beam to study each junction of our structure lets us create PN junction models (called Subckt_Iph_diode) which contain a voltage-controlled current source. The amplitude value of this current source is defined by I_{ph} as expressed in Eq. (1):

$$I_{ph} = \frac{1}{\gamma}(a\,V + b)\alpha_{gauss}\; Pulse_{width}\; W_{coef}\; I_{ph\_z} \tag{1}$$

where, V is the reverse-biased voltage, a and b depend on the laser power, γ is an amplitude attenuation coefficient, α_{gauss} is the sum of two Gaussian functions which take into account the spatial dependency, $Pulse_{width}$ considers the laser pulse duration dependency, W_{coef} is an exponential function allowing for the wafer thickness effect and I_{ph_z} is a curve function which considers the focus effect of the z axis of the laser lens:

$$\alpha_{gauss} = \beta\, e^{\left(\frac{-d^2}{c_1}\right)} + \rho\, e^{\left(\frac{-d^2}{c_2}\right)} \tag{2}$$

$$Pulse_{width} = 1 - e^{\left(\frac{-t_{pulse}}{250\cdot 10^{-9}}\right)} \tag{3}$$

$$W_{coef} = e^{-0.001\;\; Wafer_{thickness}} \tag{4}$$

$$I_{ph\_z} = (c_1 z^6 + c_2 z^5 + c_3 z^4 + c_4 z^3 + c_5 z^2 + c_6 z + c_7) c_8\, e^{\frac{-z^2}{20.000}} \tag{5}$$