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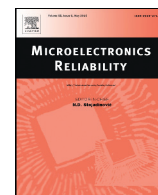

Latent gate oxide defects case studies

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ABSTRACT

Gate oxide rupture is a major concern in IC failure reliability, especially as latent wafer fab defect is difficult to screen out at component testing. Failure Analysis is key in improving product quality as it allows understanding the failure root cause in order to establish manufacturing corrective actions. Three automotive components Failure Analysis cases dealing with different types of latent gate oxide defects will be presented as well as the associated correctives actions.

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1. Introduction

The Wafer Fab defectivity improvement is strongly dependent on the Failure Analysis conclusions, hence the accuracy of the electrical and the physical characterization steps is primordial. On majority of silicon semiconductor technologies, the gate oxide ruptures are yield and reliability limiting defects. Indeed a defect in this thin dielectric layer can induce several failure modes such as functional failure, short or leakage. Different electrical and physical analysis techniques can be used to characterize this type of defect. Also, it impacts qualification results with ELFR or Burn-In rejects, yield loss as well as customer Field Failure returns. Potentially, those defects can occur on any single MOS transistor or capacitor, and is not necessarily screened with the test coverage (latent defect). Three cases studies dealing with latent gate oxide wafer fab defect are described.

2. Micro-scratch defect

2.1. Electrical and physical characterization

Different physical analysis approaches can be used to characterize micro-scratch defects. The first consists of deprocessing the die straight down to Silicon level by using hydro fluoric acid (HF). This technique applied to a defective part returned by customer allowed to highlight several similar silicon scratches in active area in the shape of “shark gills” as illustrated in Fig. 1. This defect was evidenced using Optical Beam Induced Resistance Change (*OBIRCh*) technique [1] which pinpointed an abnormal resistance change inside the leaky MLD0 MOS transistor. The presence of these anomalies at Silicon level has weakened gate oxide layer and induced its rupture at customer level.

The second physical approach performed with Focused Ion Beam (FIB) cross section on field customer return allowed a clear understanding of the origin of the wafer fab issue. This part presented a functional failure (wrong voltage on VCC5) and was analyzed by Emission Microscopy (*EMMI*) technique [2] to localize a defective area on C2 capacitor (short failure) (see Fig. 2). FIB cross-section at this location evidenced a Wafer Fab issue in the Shallow Trench Isolation (STI): STI scratches (see Fig. 3) [3]. This defect explained the capacitor short failure.

In summary, improper STI polish step is responsible of micro-scratch:

– First case showed micro-scratch at silicon active area
– In second case STI scratch are directly responsible of this defect.

2.2. Failure root cause and correctives actions

For the several cases analyzed, the failure root cause is a latent defect not screened at Probe nor Final Test.

For micro scratch defect, investigations showed that the process step responsible for these STI and active area scratches is correlated to particle defectivity during Chemical Mechanical Polishing (CMP) process [4]. On CMP Tool during STI polish process, polish pad spins and polish head will lower the wafer (with top surface facing down) towards the pad to be polished. The process is accomplished by polishing slurry consisting of colloidal silica suspended in a KOH solution. Once packed into the polish pad, the silica particles agglomerate and then scratch the surface of the wafer causing damage (see Fig. 4). Consequently, by reducing

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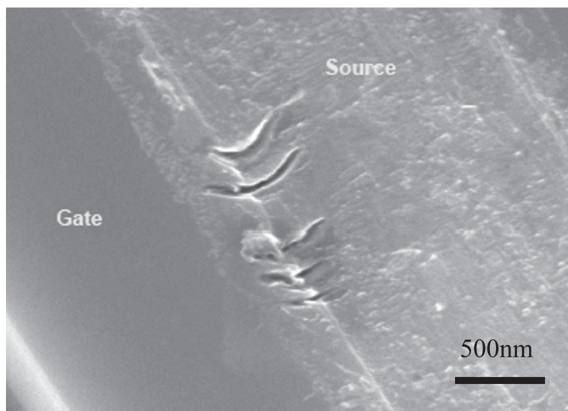

Fig. 1. SEM picture: Silicon "shark gill" microscratches.

particle defects in the CMP process, the probability of micro scratch defectivity will be reduced.

Two correctives actions were implemented:

1) Improve polish pad conditioner cleaning by converting spray nozzles to lower flow with higher velocity, which reduces probability of fall-on particle to the polish pads.
2) Implement global irrigation flow control which reduces splash-back of debris onto the polish pads.

Wafer fab evaluation data showed 50% particle reduction with the CMP improvements compared to the current process. Such improvements cannot guarantee zero defect but they contribute efficiently to reduce the defect recurrence. These CMP improvements have been implemented on applicable tool sets.

3. Recurrent capacitor corner gate oxide rupture

3.1. Electrical and physical characterization

Several customer returned parts presenting a functional failure (wrong voltage on VCCP) were characterized by EMMI technique which highlighted a defective area on the very same capacitor corner. Also OBIRCh technique under probe needle was applied for a second part (C1 capacitor leakage failure) which gives the same defect location (see Fig. 5).

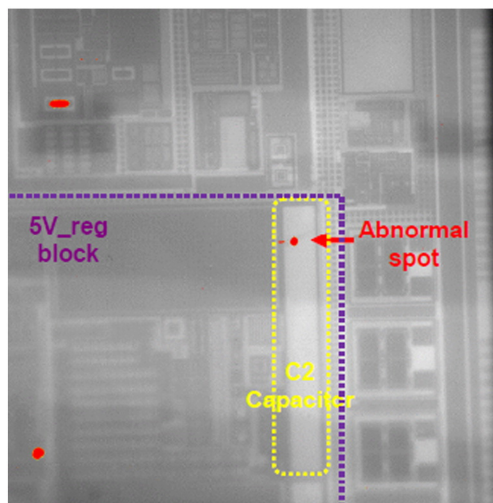

Fig. 2. Backside EMMI localization on C2 Capacitor.

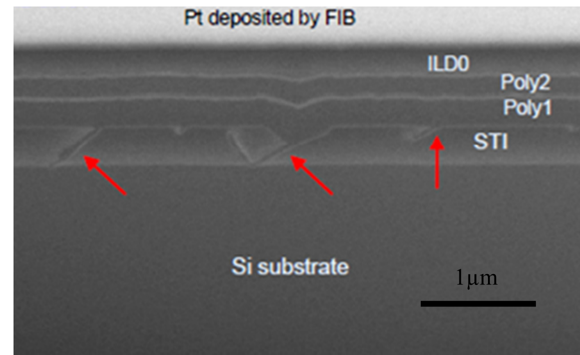

Fig. 3. FIB cross section: STI micro_scratches.

For these devices, another physical approach being applied consists of deprocessing the part step by step and then observing the gate oxide after etching chemically the polysilicon layer. It allowed to evidence a gate oxide rupture exactly at the corner of the capacitor as located by the EMMI and OBIRCh techniques (see Fig. 6). Since recurrent customer returns have been received, it was decided to change the physical characterization approach by performing a deprocessing straight down to silicon level. This technique confirmed the presence of the dielectric rupture but also highlighted at this capacitor corner location abnormal Silicon pits (see Fig. 7). These Silicon surface anomalies have weakened the gate oxide at this location.

3.2. Failure root cause analysis and correctives actions

Wafer fab investigations have shown that the sacrificial Nitride layer used to protect Silicon Active Area during STI CMP process was thinned down at this capacitor corner, dice from wafer edge were subject to these phenomena. This can be explained by the layout configuration, indeed, Active Area density is low at this location, affecting locally CMP removal rate. Then, it is highly suspected that hot phosphoric acid used to remove the sacrificial Nitride layer is in contact with Silicon Active Area for a too long time, as nitride is thinner at this location, leading to the creation of Silicon pits.

First containment action was to bin out the dice from the wafer edges, meanwhile investigations on modifying CMP and nitride etch parameters are ongoing. Such changes are delicate due to lack of CMP removal rate homogeneity over the wafer surface. Finally, adding dummies structures are considered in order to increase Active Area density at this location.

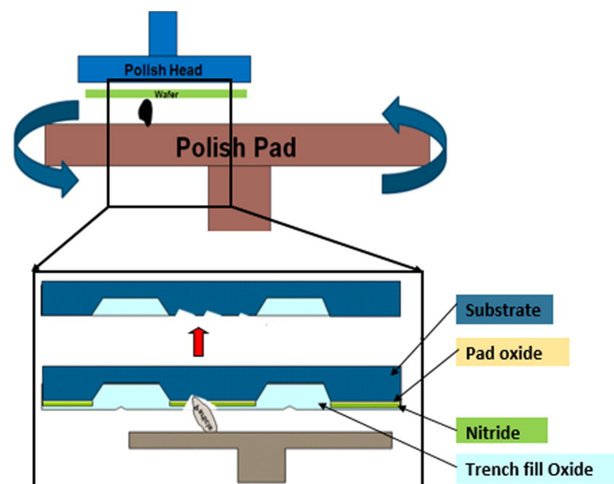

Fig. 4. Microscratch defect formation principle.

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