

# Fault isolation in a case study of failure analysis on Metal–Insulator–Metal capacitor structures

V. Giuffrida, P. Barbarino, G. Muni, G. Calvagno, G. Latteo, D. Mello \*

STMicroelectronics Stradale Primrose 50, 95121 Catania, Italy



## ARTICLE INFO

### Article history:

Received 25 May 2015

Received in revised form 20 June 2015

Accepted 20 June 2015

Available online 30 June 2015

## ABSTRACT

Metal–Insulator–Metal (MIM) capacitors are extensively used in many microelectronic products such as BICMOS for automotive radar applications, but failure analysis process is very laborious due to peculiar structure. In this paper a possible fault isolation process flow was shown in a failure analysis case study. In particular due to the fact that it is a customer return device, many checks were done in fault isolation steps before physical analyses. Finally a FIB cross section was performed on OBIRCH hot spot and the results confirmed the validity of the fault isolation process.

© 2015 Elsevier Ltd. All rights reserved.

## 1. Introduction

The high density capacitors are extensively used in many products and microelectronic devices such as RF devices in BICMOS technology used for automotive radar applications. Often they can be obtained using Metal–Insulator–Metal (MIM) capacitors, which can use thin insulators with high dielectric constant and can be connected in large batteries and stacked with standard capacitors as well [1,2].

Failure analysis process on these particular structures is very laborious due to peculiar structure and MIM's manufacturing complexity. The simultaneous presence of large areas, ultra-thin oxide, topmost layers involved, etc. complicates very much the physical inspection in order to find defects and route causes.

In the past, it has been shown a sample preparation method to prepare and observe the untouched dielectric oxide, which is very useful in many real cases of failure analysis, in particular if you are searching thin oxide cracks [3].

However there are many other cases in which, the large area of the condenser in contrast with the small dimension (few nanometers) of the defect makes impossible to find and observe the failing cause. At the same time MIMs are connected in batteries in order to increase capacity, making therefore complicated the localization of the failure by fault isolation.

The aim of this work is to present a different approach consisting in fault isolation and FIB cross-section than previous de-processing based methodology [3]. In particular the process steps used to obtain a reliable hot spot will be illustrated.

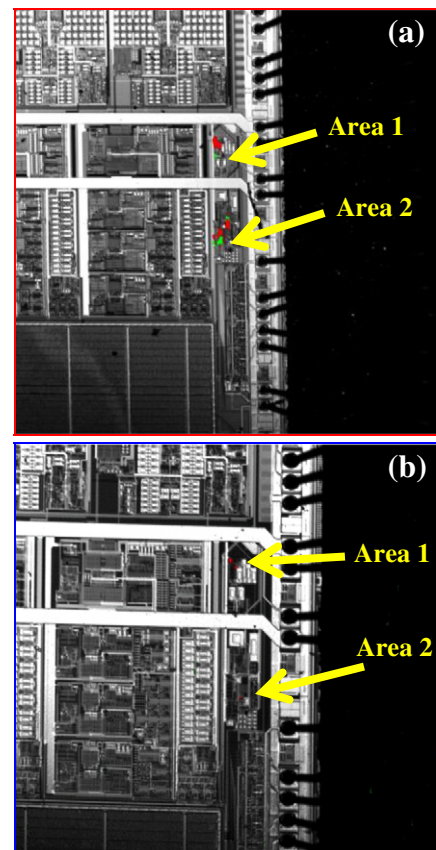


Fig. 1. Overview of OBIRCH superimposed image of fail device (a) vs good (b).

\* Corresponding author.

E-mail address: [domenico.mello@st.com](mailto:domenico.mello@st.com) (D. Mello).

## 2. Experimental

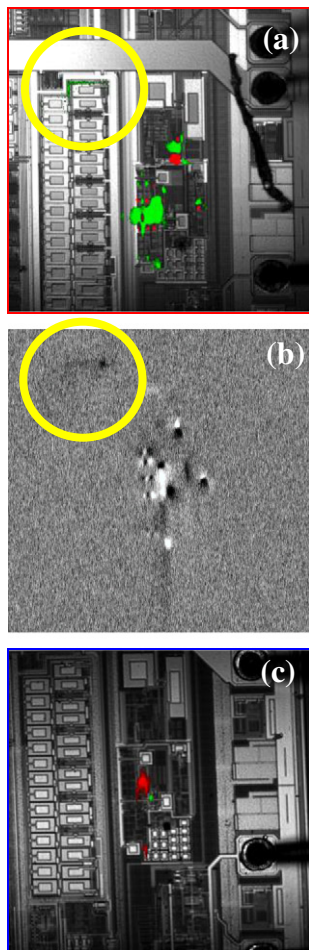
Fault isolation was performed using a Hamamatsu Phemos 1000 equipped with a laser YLF with a  $\lambda = 1.3 \mu\text{m}$  in order to achieve Optical Beam Induced Resistance Change (OBIRCH) operative set-up.

Cross sections were performed using a Focused Ion Beam (FIB) of Dual Beam Zeiss XB 1560 equipped with a field emission source in the electronic column and a Ga LMIS in the ion column. Furthermore the system is equipped with a GIS used to deposit platinum, tungsten or oxide.

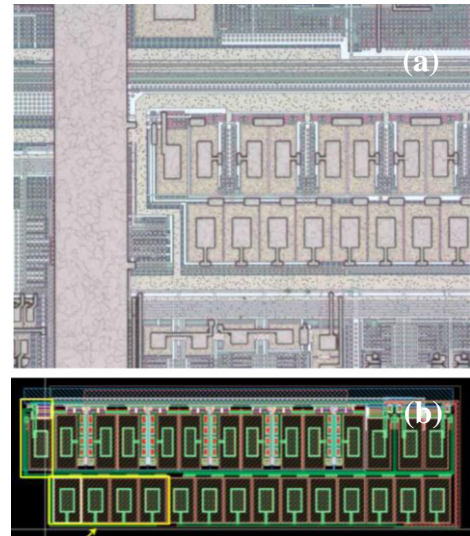
## 3. Results and discussion

This case study is based on a customer return device in which an anomalous current sink was found after some hours of operation on the application board. The area of the failing block into the device is largest and the delayering previously described [3] is unable to find any defects. An alternative approach would be to insulate each condenser, cutting by FIB the metal of the interconnection. But because we would like to correlate the defect to the electrical signature, the classical approach with fault isolation was done.

Failure analysis flow was designed to insulate and observe the defect. The starting point was the electrical analysis on Automatic Test Equipment (ATE). For this step the standard approach to verify a failure is to test the component on the ATE with the test program used in production.



**Fig. 2.** Details of the areas signed as Area 2 (Fig. 1). In particular the fail device (a), with his OBIRCH image (b) vs the good one (c) is reported.



**Fig. 3.** Detail of the area indicated from OBIRCH (a) and layout of the same area (b).

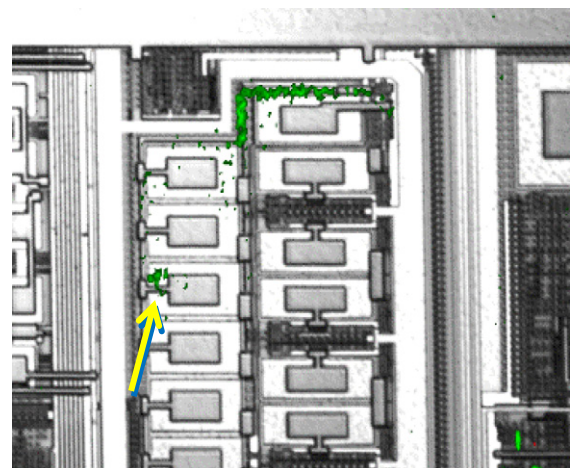
The advantages of using the ATE to verify the failure are:

1. The validation is correlated with production standards.
2. The ATE can give a datalog of results for each parameter, identifying the specific failure.

Test stability and repeatability must be ensured to detect non-stable defects.

The results of ATE are evaluated in order to understand which macro-electrical failure mode may be simulated at bench for fault isolation. Typically these returns are not affected by continuity faults and the electrical failure mode is due to an anomalous consumption from some power supply line in applicative conditions. So after ATE confirmation, we verify at bench the anomalous consumption related to one or more power supply lines once the device is completely powered up.

Once we have found one setup in which an anomalous overcurrent is observed we submit the unit to decap and then we perform OBIRCH analysis under applicative conditions. In particular we supply through OBIRCH only supply line showing the anomalous consumption while we externally supply all other signals. Among all the hot spot found, the most promising superimposed image is shown in Fig. 1. In this figure, two areas, signed as Area 1 and Area 2, appeared immediately interesting.



**Fig. 4.** Zoomed in OBIRCH image of the defective MIM battery.

Download English Version:

<https://daneshyari.com/en/article/6946695>

Download Persian Version:

<https://daneshyari.com/article/6946695>

[Daneshyari.com](https://daneshyari.com)