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Compact thermal modeling of spin transfer torque magnetic tunnel junction

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ABSTRACT

Magnetic tunnel junction (MTJ) with spin transfer torque (STT) switching method features fast speed, low power, great scalability and high compatibility with conventional CMOS process. Nevertheless, its magnetic and electrical properties can be easily influenced by operation temperature and self-heating effect, which further results in performance degradation and reliability issues of MTJ based memories and logic circuits. This paper investigates the behaviors of MTJ under different temperatures and further proposes a model in consideration of temperature impact on performance of MTJ, which can be used to optimize the design of STT-MRAM in terms of dynamic operations and temperature tolerance.

1. Introduction

Spin transfer torque magnetic tunnel junction (STT-MTJ) is the essential element of STT magnetic random access memory (MRAM), which is a promising candidate of non-volatile memory owing to its attractive performances, e.g. high speed operation (~10 ns for writing and ~200 ps for reading), low power consumption, infinite endurance and great miniaturization perspective (<22 nm) [1]. Recent research demonstrates that MTJ with perpendicular magnetic anisotropy (PMA) has achieved larger thermal stability, lower switching current density and faster access speed than that with in-plane magnetic anisotropy (see Fig. 1) [2].

However, several magnetic properties of MTJ are sensitive to temperature fluctuation, e.g. anisotropy field, magnetization of ferromagnetic layers [3,4]. This leads to the unsteadiness of electrical properties of MTJ such as tunneling magnetoresistance ratio (*TMR*), thermal stability factor Δ, critical switching current I_{c0}, as well as switching delay τ and further results in operational failures. Thus, as one of the major causes of stochastic STT switching, the initial temperature variation also has an important impact on data retention [5]. Furthermore, most of the STT switching operations require a high current density flowing through the MTJ [6], which generates a temperature increase due to Joule heating [7]. Therefore, a thorough study of high-temperature behaviors of MTJ is always required for reliability aware design of MTJ/CMOS circuits.

This paper proposes a model of STT PMA MTJ taking into account high temperature behaviors and the self-heating effect. As typical industrial temperature range is from −40 °C to 125 °C, the simulations in this work will consider temperatures between 233 K and 400 K. In Section 2, the model including temperature sensitive parameters will be presented. Section 3 will focus on the temperature impact of MTJ based CMOS circuits, followed by the conclusion.

2. Model of temperature sensitive parameters

This section concentrates on the impact of temperature on tunneling magnetoresistance ratio (*TMR*), thermal stability factor Δ, critical switching current I_{c0} and switching delay τ. Indeed, the strong temperature dependence of *TMR*, I_{c0} and τ have been observed in many research investigations [10,11], which influence deeply the characteristics of MTJ at different temperature conditions, whereas Δ can be deduced theoretically.

2.1. Temperature dependence of TMR

Experimental results show that resistance at antiparallel state reduces faster with temperature increase than that at parallel state, which originates from the degradation of *TMR* [12]:

$$TMR\,(T) = (TMR_0 + 1)/\left(1 + 2Q \cdot \beta_{AP} \cdot \ln\left(\frac{k_B T}{E_c}\right)\right) - 1 \tag{1}$$

where TMR_0 is at zero temperature, E_c is the magnon energy cutoff energy, Q describes the probability of a magnon involved in the

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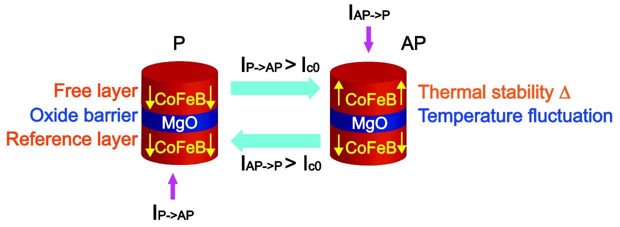

Fig. 1. Main structure of MTJ consists of three layers: two ferromagnetic layers separated by an oxide barrier. The nanopillar resistance (R_p, R_{ap}) depends on the corresponding state of the magnetization of the two ferromagnetic layers parallel (P) or anti-parallel (AP) [8]. The resistance difference is characterized by tunnel magnetoresistance ratio TMR = (R_{ap}-R_p) / R_p [9]. With spin transfer torque mechanism, MTJ changes between two states when a bidirectional current I is higher than the critical current I_{c0} [1]. The main provenance of temperature fluctuation is oxide barrier and the thermal stability factor is mainly determined by free layer.

tunneling process, $\beta_{AP} = Sk_BT/E_m$, S is the spin parameter, while E_m is related to the Curie temperature of the ferromagnetic electrodes $E_m = 3k_BT_C/S + 1$.

In addition, *TMR* is also dependent on bias voltage [13]:

$$TMR\ (V) = TMR\ (0,T)\cdot\left(1+\frac{V^2}{V_h^2}\right)^{-1} \tag{2}$$

where *TMR*(0,*T*) is at zero bias, V_h is a voltage for which *TMR* becomes half of *TMR*(0,*T*). Thus, a complete model of *TMR* can be deduced:

$$TMR\ (V,T) = TMR\ (T)\cdot\left(1+\frac{V^2}{V_h^2}\right)^{-1}. \tag{3}$$

Fig. 2 displays the temperature dependence of *TMR*, which is consistent with the experimental results [12].

2.2. Temperature dependence of thermal stability factor Δ and data retention

Thermal stability factor Δ is often used to quantify the reliable data retention of magnetic data storage [14] and its value should be as large as possible to ensure a low reading failure rate. It can be calculated as follows:

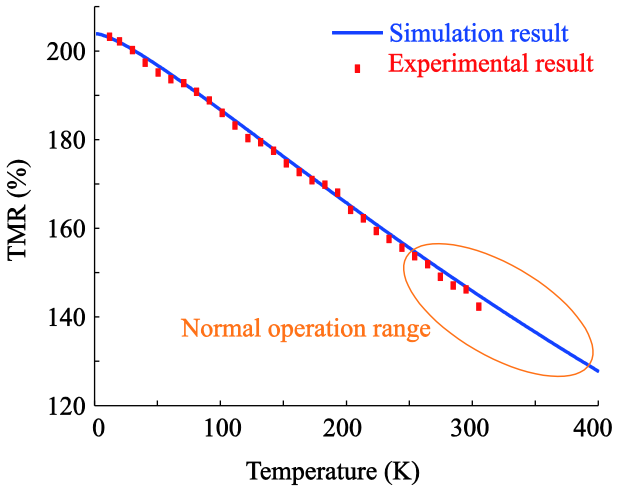

Fig. 2. TMR evolution with temperature increase and the experimental data (red points) in [12].

$$\Delta = \frac{E}{k_B T} \tag{4}$$

$$E = \frac{\mu_0 M_s \times H_K \times V}{2} \tag{5}$$

where E is the barrier energy, k_B is the Boltzmann constant, μ_0 is the permeability of free space, M_s is the saturation magnetization, H_K is the effective anisotropy field, and V is the volume of the free layer.

The impact of reading operation on the required Δ while keeping an acceptable failure rate of MTJ based memory can be expressed as follows [15]:

$$F_{chip} = 1-\exp\left[-N\frac{\tau_r}{\tau_{r0}}\exp\left(-\Delta\left(1-\frac{I_R}{I_{c0}}\right)\right)\right] \tag{6}$$

where F_{chip} is the switching error rate due to the cell read current I_R, N is the number of bits per word in the memory array, τ_{r0} is the attempt period = 1 ns and τ_r is the accumulated read duration.

Fig. 3 demonstrates that effective anisotropy filed H_k and saturation magnetization M_s decrease with increasing temperature and the simulation results show good agreement with experimental data in [4]. This results in the deep temperature dependence of Δ as shown in Fig. 4. The chip failure rate of 8 bit per word with different reading duration ratios in data retention (1% or 10%) and different ratios of read current/critical current (1/5 and 1/15) are also presented in Fig. 4. We can conclude that high temperature reduces read duration and the read current.

2.3. Temperature dependence of critical current I_{c0}

Depending on the magnitude of switching current, the switching behavior of MTJ can be divided into two regimes [16]: Sun model ($I > I_{c0}$) [17] and Neel–Brown model ($I < I_{c0}$) [18]. For PMA STT MTJ, these two regimes are isolated by the critical current which can be described by the following equations [2]:

$$I_{c0} = \alpha\frac{\gamma e}{\mu_B g}(\mu_0 M_s)H_K V = \frac{2\alpha\gamma e}{\mu_B g}E \tag{7}$$

where α is the damping constant, γ the gyromagnetic ratio, e is the elementary charge, μ_B is the Bohr magneton, and $g = \sqrt{TMR(TMR+2)}/2(TMR+1)$ is the spin polarization efficiency factor. Thus, critical switching current I_{c0} has strong temperature dependence (see Fig. 5). The mechanism behind this phenomenon is as follows: as temperature

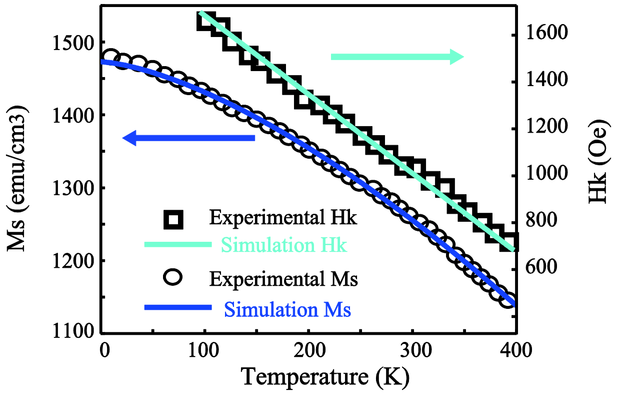

Fig. 3. Temperature dependence of effective anisotropy field H_k and saturation magnetization M_s.

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