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Investigation of the dynamic on-state resistance of AlGaN/GaN HEMTs

M. Rzin [a,*], N. Labat [a], N. Malbert [a], A. Curutchet [a], L. Brunel [b], B. Lambert [b]

[a] IMS Laboratory, University of Bordeaux, 351 Cours de la libération, Talence, France
[b] United Monolithic Semiconductor, 10 Avenue du Québec, 91140 Villebon-sur-Yvette, France

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ABSTRACT

The dynamic on-state resistance (R_{ON}) increase in AlGaN/GaN high-electron-mobility transistors (HEMTs) has been investigated by pulsed I–V measurements on devices issued from UMS GaN technology. We have studied the influence of the measurement setup on the pulsed I–V measurements and highlighted the importance of the $I_{DS}(t)$ waveforms to verify the validity of the measurements. The R_{ON} is not sensitive to short time transients below 10 μs as well as for fresh and HTRB aged devices. The dynamic resistance (R_{ON}) is doubled in off-state conditions by increasing V_{DS0} from 0 V to 50 V. The threshold voltage V_{TH} of aged devices has not shifted during the HTRB aging test carried out for 2200 h. Therefore, trapping effects responsible for the increase of R_{ON} are rather more located in the gate-source and drain–source access regions than under the gate.

1. Introduction

The GaN HEMT presents great interest and is a very promising device for microwave and power electronics applications [1] and also for high temperature wireless sensors [2]. This is in great part due to the physical and electrical properties of the AlGaN/GaN heterostructure: high breakdown electric field, high electron mobility and good thermal conductivity. Another significant feature is the high thermal conductivity of SiC substrate [3]. These characteristics enable very high frequency switching operations allowing the GaN HEMT to be a competitive device with the dominant power devices. However, trapping effects are still limiting the performances of GaN based HEMTs.

The most critical parameter for high voltage switching is the dynamic on-state resistance R_{ON} that increases for high switching frequency. The study of the evolution of the dynamic on-state resistance R_{ON} during pulsed *I–V* measurements depending on the quiescent bias conditions is the subject of many research studies [4–7].

In this work we highlight the dependence of the pulsed I–V characteristics and of the dynamic on-state resistance R_{ON} on the measurement setup. Moreover, insight is given on the $I_{DS}(t)$ waveforms to verify the validity of the pulsed I–V measurements. The high field induced trapping effects in off-state conditions are studied by investigating the R_{ON} increase in off-state conditions. High Temperature Reverse Bias (HTRB) aging test was carried out for 2200 h in order to give more insight on the physical location of trapping effects causing R_{ON} variation.

In the following section, we briefly describe the studied GaN based HEMT technology. The third section is dedicated to the pulsed measurement setup. The fourth section describes the conditions of the pulsed measurements and highlights the importance of the $I_{DS}(t)$ and $V_{DS}(t)$ waveforms to verify the validity of the I–V pulsed measurements. In the last section, we discuss the evolution of R_{ON} during pulsed I–V measurements for fresh and aged devices.

2. Technology description

The GH25 qualified technology [8] is based on an AlGaN/GaN epitaxy on SiC substrate with a 0.25 μm Au based gate metal. The AlGaN layer is about 20 nm thick. This technology intends to cover high power and wide band frequency applications up to Ku band for telecom and defense markets. Studied AlGaN/GaN HEMTs present 8 × 125 μm gate finger topology, standard ohmic contacts, a silicon nitride passivation and a source terminated field plate and gate drain distance of 1.7 μm. Virgin samples used as reference devices, as well as aged devices were characterized by pulsed I–V measurements. Four samples have been submitted to High Temperature Reverse Bias (HTRB) aging test carried out at $V_{GS} = -7$ V and $V_{DS} = 50$ V for 2200 h with a channel temperature T_{CH} of 175 °C. This test is used to assess the gate contact stability.

* Corresponding author.

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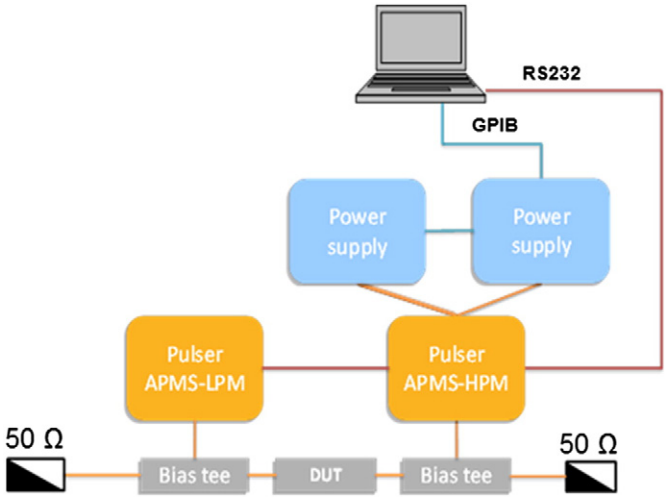

Fig. 1. Pulsed I–V measurement setup.

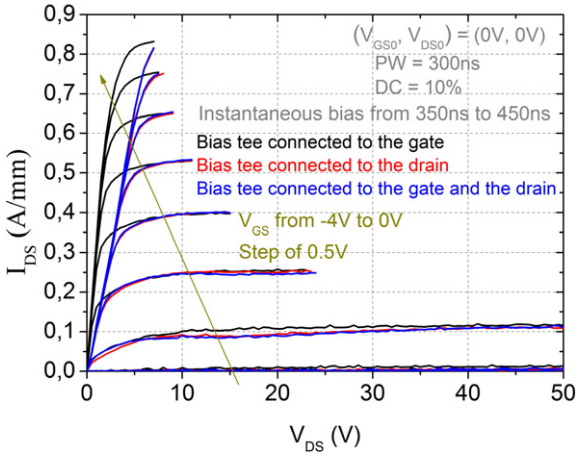

Fig. 2. Pulsed I–V measurements at (V_{GS0}, V_{DS0}) = (0 V, 0 V), connecting the bias tee on the gate (black line) or the drain (red line) or both (blue line).

3. Pulsed I–V measurement technique

The measurement system (developed by MC^2 Technologies) is shown in Fig. 1.

It is supplied with two pulsed heads, one dedicated for high voltage and high current suitable for the drain–source pulse and sense (APMS-HPM) and the second one designed to reach high accuracy in lower voltage and current suitable for the gate-source pulse and sense (APMS-LPM). Two external power supplies are needed to bias the drain.

The bias tees are generally used to perform the S-parameters measurements in pulsed mode and also to stabilize the component by avoiding oscillations. We have studied the influence of the bias tees on the pulsed I–V measurements. The used bias tee is a KEYSIGHT 11612A that operates in the frequency range of 45 MHz–26.5 GHz.

4. Pulsed I–V measurements

The pulsed I–V measurements were carried out at different quiescent bias (*QB*) conditions (V_{GS0}, V_{DS0}) to quantify the gate and drain lag phenomena. The waveforms $V_{DS}(t)$ and $I_{DS}(t)$ were extracted to verify the stability of the quiescent and instantaneous biases of the device; as a consequence, it is ensured that instantaneous measurements are performed in the time window within which $V_{DS}(t)$ and $I_{DS}(t)$ are stable. A pulse width (*PW*) of 300 ns is used to study the lag phenomena and the dynamic resistance R_{ON}.

Fig. 2 shows 300 ns pulsed I–V measurements of a representative fresh device using the quiescent bias condition (V_{GS0}, V_{DS0}) = (0 V, 0 V) with a duty cycle of 10% while connecting a bias tee on the gate or the drain or both electrodes. To minimize noise and enhance measurement accuracy, an average of 1024 measurements is performed. This figure shows that the use of a bias tee connected on the drain induce measurement artifact on the I–V pulsed measurements. Furthermore, when removing the bias tees on both the gate and the drain, we obtain the same results as when the bias tee is connected only on the gate.

Fig. 3 shows typical $I_{DS}(t)$ waveforms for the quiescent bias condition (V_{GS0}, V_{DS0}) = (0 V, 0 V) at V_{GS} = 0 V for V_{DS} from 0 to 7 V.

The quiescent bias (QB) is measured from 50 ns to 150 ns, and the instantaneous bias (IB) is measured from 350 ns to 450 ns. When the bias tee is connected only on the gate, the $I_{DS}(t)$ waveform is steady in the instantaneous bias window for the whole instantaneous bias V_{DSi} range. On the other hand, when the bias tee is connected only on the drain, the $I_{DS}(t)$ waveforms are not steady in the instantaneous bias window. Thus, the noticeable increase of R_{ON} in Fig. 2 is due essentially to capacitive and inductive effects of the bias tee.

Fig. 4 shows pulsed I–V measurements at (V_{GS0}, V_{DS0}) = (0 V, 0 V) and pulse width of 300 ns, 1 μs and 10 μs and a duty cycle of 10% at V_{GSi} = 0 V with the bias tees connected on the gate and the drain and *dc* I–V measurement at V_{GS} = 0 V. The slope of pulsed I_D vs. V_{DS} increases by increasing the pulse width from 300 ns to 10 μs. Thus, R_{ON} decreases by increasing the pulse width to achieve the value of R_{DS} at *PW* = 10 μs.

Jin and Del Alamo ([5] and [6]) have reported on the rise of the slope of I_D vs. V_{DS} by increasing the pulse width from 200 ns to 1 ms. They

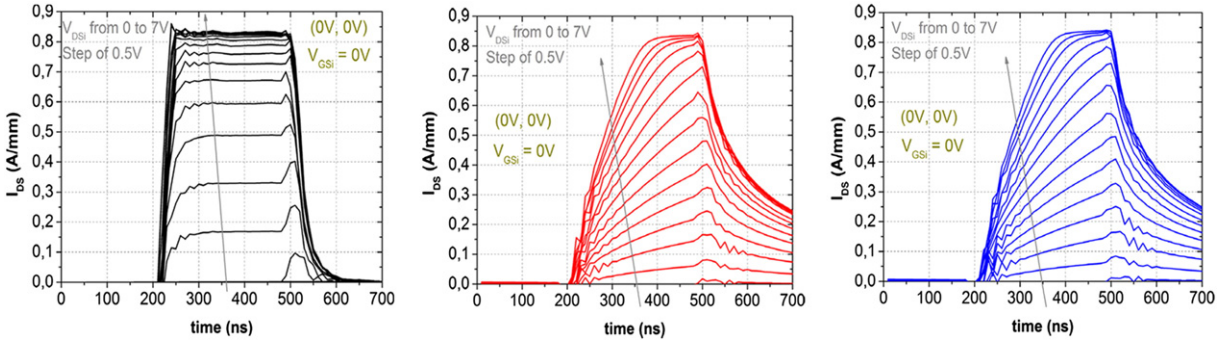

Fig. 3. $I_{DS}(t)$ waveform measured by pulsed I–V measurement setup with bias tee connected on the gate only (left plot in black) or the drain only (center plot in red) or both (right plot in blue). Measurement conditions: (V_{GS0}, V_{DS0}) = (0 V, 0 V), pulse width (PW) = 300 ns, duty cycle (DC) = 10%.