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As-grown donor-like traps in low-k dielectrics and their impact on intrinsic TDDB reliability

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ABSTRACT

Highly porous low-k dielectrics are essential for downscaling of the interconnects for 20–10 nm technologies. A planar capacitor test vehicle was used to investigate the intrinsic time dependent dielectric breakdown (TDDB) reliability of low-k dielectrics and the origin of an observed *C–V* hysteresis was studied. We hypothesize that the hysteresis is caused by donor-like traps present in the bulk of the low-k but not by electron/hole trapping or mobile charges. It is proposed that porogen/carbon residues are the source of these donor-like traps. Using I_{leak} vs. time measurements, it was found that the donor-like traps accelerate the dielectric degradation due to an enhanced E_{OX}, causing a localized partial breakdown. The intrinsic TDDB reliability of the low-k film was improved by adding a sealing layer as such layer blocked the donor-like traps discharging.

1. Introduction

The application of low-k materials in back-end-of-line (BEOL) as inter-metal dielectric (IMD) layer is essential for downscaling of the interconnects for 20–10 nm technologies [1,2]. As dielectric spaces and k-values decrease, the time dependent dielectric breakdown (TDDB) becomes one of the most critical reliability issues for the Cu/low-k interconnect systems. One of main extrinsic cause is Cu penetration due to the poor barrier, which leads to early TDDB failure [3]. In order to evaluate the reliability properties of low-k materials, it is important to study their intrinsic breakdown behaviour [4,5]. It is well known there is a strong link between that the intrinsic TDDB performance and the traps in gate oxide [6]. So far, however, there are limited studies on the relationship between traps and TDDB in low-k materials. In order to extend the knowledge of the intrinsic TDDB of low-k dielectrics, a planar capacitor (Pcap) test vehicle was used. Compared with standard damascenes structure, the Pcap is used to investigate the intrinsic TDDB reliability of low-k materials, excluding the other extrinsic effects due to different process issues: line-edge-roughness, CD variations, low-k patterning damage, residues after chemical mechanical polishing (CMP) and so on [7–9].

In this paper, the origin of observed *C–V* hysteresis and their impact on the intrinsic TDDB reliability of low-k materials were studied by the Pcap structure. For the first time, we hypothesize that the hysteresis is caused by donor-like traps present in the bulk of the low-k. The discharged donor-like traps accelerate the dielectric degradation due to an enhanced E_{OX}. This paper is organized as follows. After a description of devices and test setup, the cause of the *C–V* hysteresis was identified and donor-like traps were attributed to porogen/carbon residues. Finally, the possible of these donor-like traps impact on TDDB and the improvement methods are discussed.

2. Device description and test setup

In this work, various dedicated capacitors to characterize low-k film properties were processed as following and summarized in Table 1. Two types of Pcaps have been used. One is metal–insulator–silicon (MIS) [4], which makes it possible to extract the flat band voltage (V_{FB}) by capacitance–voltage (*C–V*) measurement. Another one is metal–insulator–metal (MIM) [3], which is used to compare the TDDB performances under positive and negative biases. Fig. 1a shows the cross section of our planar capacitor test vehicle. The investigated organo-silicate glass (OSG) dielectrics

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Table 1
Details of the samples used in this paper.

Sample	Pcap	Low-k	Thickness	RP	UV	Sealing layer
S1	MIS	OSG 2.3	40 nm	No	Yes	No
S2	MIS	OSG 2.0	90 nm	110s	Yes	No
S3	MIS	OSG 2.0	90 nm	720s	Yes	No
S4	MIS	OSG 2.5	60 nm	No	Yes	No
S5	MIS	OSG 2.4	56 nm	No	Yes	No
S6	MIM	OSG 2.3	40/60 nm	No	Yes	No
S7	MIM	OSG 2.3	40 nm	No	Yes	12 nm OSG 3.0

with k-values between 2.5 and 2.0, were deposited by plasma enhanced chemical vapor deposition (PECVD) onto a n-type Si substrate (MIS) or 10 nm TiN layer (MIM). In order to minimize the interfacial effects between the substrate and the low-k, 1 nm SiO_2 layer was thermally grown onto n-Si before low-k deposition for MIS Pcap. In case the copper ion penetrate into low-k materials, a 4 nm PVD TaN/Ta layer was deposited between low-k and Cu. In order to remove the porogen, various treatments including remote plasma (RP) healing and UV assisted thermal curing have been done after low-k deposition [8]. In the interest of blocking the potential donor-like trap discharging, a sealing layer was deposited prior to the metal deposition for S7. More process details are introduced in [3,4,7]. The area of capacitor is 100 μm × 100 μm.

The V_{FB} shift was obtained from high frequency *C–V* (HF *C–V*) measurements which were performed using a HP4284A Precision LCR Meter. TDDB experiments were carried out using a HP4142B Modular DC Source at 100 °C under various electric fields. An abrupt increase in leakage current was used as the failure criterion of dielectric breakdown.

3. Results and discussion

3.1. Typical test results

A double direction *C–V* with bias sweeping between +1 MV/cm and −1 MV/cm was performed on the MIS-samples, as shown in Fig. 1b. *C–Vs* show a hysteresis, where the flat band voltage shift depends on the used low-k. For instance, as indicated on Fig. 1b, one observed a 0.6 V V_{FB} shift on sample S1.

The origin of this hysteresis effect could be (a) electron (e−) trapping, (b) hole (h+) trapping, (c) mobile charges or (d) as-grown traps in the bulk of low-k materials. Each possibility is examined below one by one. As discussed in Fig. 2, the V_{FB} is changed under different bias conditions. including (a) under positive bias, the electron trapping from substrate leads to the increase of V_{FB}. It is also possible that the traps discharge into metal side, resulting in V_{FB} decrease; (b) under negative bias, the electrons trapping from metal also leads to the increase of V_{FB}. Whilst, the traps discharge into substrate side or hole trapping from substrate make V_{FB} decrease; (c) in terms of the movement of mobile charges, the mobile positive charges moves to substrate under positive bias, which causes V_{FB} decrease, and vice versa under negative bias.

3.2. Evidences against the other possibilities

Fig. 3a shows that the V_{FB} shift becomes more negative with stress time under a positive stress *V*. This observation excludes the possibility of electron trapping from the Si-substrate, as the V_{FB} should increase in this case (Fig. 2a). Fig. 3b further confirms that the electron trapping is insignificant as the negative V_{FB} shift dominates even at low stress voltages. Quasistatic *C–V* confirms

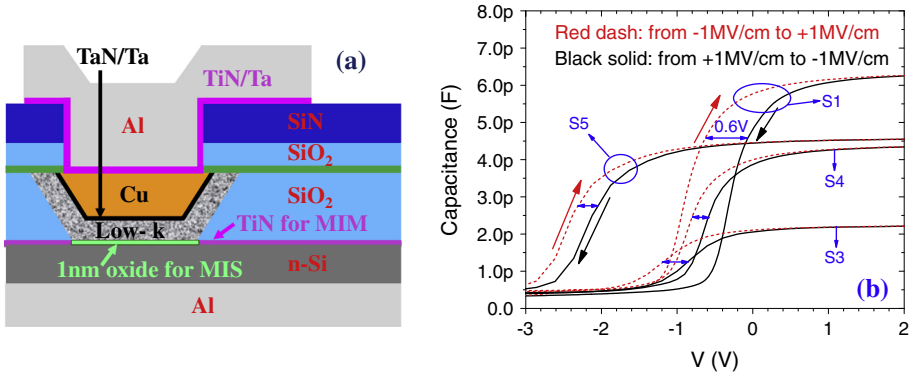

Fig. 1. (a) Schematic cross section of MIM/MIS Pcap. A 10 nm TiN layer below the low-k was deposited in MIM Pcap, which replaced the position of 1 nm SiO_2 in MIS structure. (b) Typical *C–V* hysteresis on various low-k materials. The biases sweep between ±1 MV/cm under the same speed for comparisons. Noted that only part of focused range in voltage are shown here.

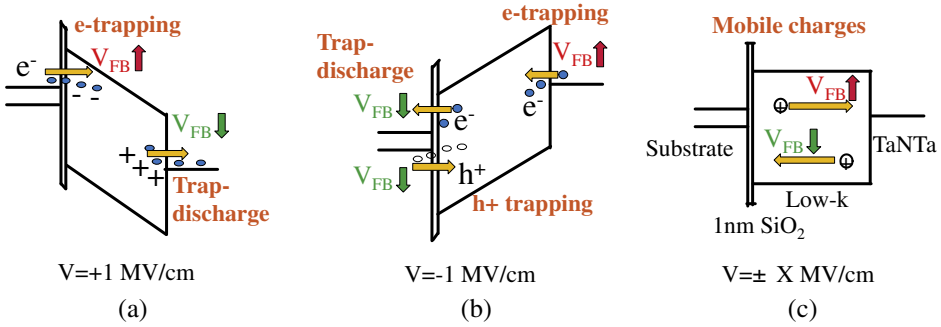

Fig. 2. Possibilities which lead to V_{FB} instability are examined at different bias conditions, as shown the illustration of energy band diagrams of Pcap (a) under positive stress voltage, (b) under negative stress voltage, (c) under alternating polarity of stress voltages.