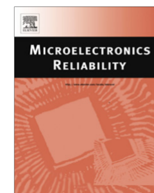
Microelectronics Reliability xxx (2014) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Physics-of-failure assessment methodology for power electronic systems

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ARTICLE INFO

Article history:
Received 27 June 2014
Accepted 16 July 2014
Available online xxxx

Keywords:
Power electronics
High temperature
Control boards
High power
Motor drives

ABSTRACT

Driven by consumer markets and industrial needs, power electronic systems are operating at higher power densities, in smaller packages and in more exotic environments. As these trends continue, ensuring long-term operation in harsher conditions requires accurate reliability prediction models, most viably obtained through Physics-of-Failure (PoF) methodologies. This paper introduces a PoF-based system-level reliability assessment procedure in which the dominant failure mechanisms are identified for three primary subsystems: the power module, DC-link capacitors and the control circuitry. This report outlines the dominant failure modes and mechanisms for each subsystem and provides examples of how to improve subsystem reliability based upon the described assessment methodology. A case study is also presented in which the solder interconnect reliability of the gate-driver board in a mid-range variable frequency drive (VFD) was assessed.

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1. Introduction

In the past decade, power electronic system development has been characterized by size, weight and performance (SWaP) optimization as well as the industry-driven requirement to operate in harsh environmental conditions. Wide bandgap semiconductor devices have facilitated these developments by enabling operation above the 175 °C application temperature limit of silicon [1–6].

In the aerospace industry electrical actuators in commercial aircraft are increasingly being driven by power electronic converters [7]. In some cases this requires placing converters near the jet engines which routinely experience deep thermal cycling from −55 °C to 225 °C [8]. Similarly, down-hole electrical gas compressors used in deep oil-well drilling may be required to operate over temperatures ranging from 150 °C to 225 °C for periods of up to 5 years [9]. Due to the high-cost of stopping production, these systems must be designed with reliability at the forefront of considerations.

While wide bandgap semiconductor devices enable converters to operate in harsher environments, minimal research efforts have been directed towards ancillary subsystems. Trends surrounding state-of-the-art integrated packaging place vital subsystems, such as the power capacitors and gate-driver circuitry, closer to the power module [10–13]. As power densities increase and system dimensions decrease these subsystems will presumably experience increased stress levels due to the additional heating from the switching and conduction losses originating from the converter. Coupled with extreme environment, therein lies the potential for ancillary subsystems to become a major reliability concern.

In order to continue the drive towards fully-integrated power electronic systems, fundamental groundwork must be established to quantitatively assess the reliability implications of a compact system architecture coupled with harsher environments. The majority of physics-of-failure based reliability efforts have been geared towards the power module [14–19]. Only limited research has been conducted using PoF-based techniques involving other major subsystems. Specifically the gate-driver circuitry has seldom been the focus of reliability research, typically included in the analysis using constant failure rates or left out completely [15,20,21]. It will be of great benefit to detail a comprehensive PoF-based plan to assess the reliability of an entire power electronic system.

2. Power module failure modes

This section addresses typical failure modes associated with power module operation. Following each failure mechanism description is a corresponding test procedure detailing the assessment methodology.

2.1. Substrate failure

Power module substrates are predominately based on Direct Bond Copper (DBC), Direct Bond Aluminium (DBA) and Active

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http://dx.doi.org/10.1016/j.microrel.2014.07.123
0026-2714/© 2014 Published by Elsevier Ltd.

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Metal Brazed (AMB) technology. Ceramic insulation layers for these substrates may consist of Al_2O_3, AlN, or Si_3N_4. The substrate metallization is conventionally Cu, but in some applications Al is used. Ni can be electroplated onto Cu to protect it from oxidation and corrosion or it can be electroplated on Al to improve the wettability and enable soldering. Thin layers of Au or Ag can be plated on top of the Ni to further improve solderability and facilitate silver sintering as an interconnect technology.

Power module substrate metallization layers should have a high thermal conductivity to assist in heat dissipation. The metallization and ceramic layers should also have high thermal conductivities to increase heat spreading, thus reducing device and overall system temperatures. Furthermore, the dielectric strength of the ceramic layers must be sufficiently high to withstand breakdown stemming from the high voltages existing in power electronic applications. Table 1 provides an overview of room temperature properties of the Al_2O_3, AlN, and Si_3N_4 ceramics used in power modules.

Al_2O_3 is used in the majority of applications because of its relatively low cost. However the low thermal conductivity of this material limits its applicability to power module systems having low energy densities and heat dissipation rates.

AlN possesses a higher thermal conductivity enabling more efficient heat transfer from the power devices, through the substrate ceramic layer and ultimately to the heatsink. Due to this advantageous property, AlN is typically the ceramic of choice for power modules with high power densities and heat dissipation. Its coefficient of thermal expansion (CTE) is closer to that of Si and SiC devices than that of Al_2O_3. This reduces thermomechanical stress in the die attach during temperature excursions.

Si_3N_4 has high a flexural strength and has a fracture toughness higher than that of Al_2O_3 (4–6 MPa $m^{1/2}$ and 2.5–4 MPa $m^{1/2}$ respectively [23]). This reduces its susceptibility to failure via cracking of the substrate ceramic. Si_3N_4 cannot be used to form DBC or DBA substrates and is limited to the AMB process, which has lower interfacial strength, making it prone to early failure by delamination of the metallization from the ceramic.

Common failure modes of power module substrates include debonding of the metallization from the ceramic and cracking within the ceramic [14]. Both originate from the CTE mismatch between the metallization (high CTE) and the ceramic (low CTE) during temperature excursion. Debonding is initiated at the metallization edge followed by continued growth of delaminated areas with subsequent cycles [24]. Crack initiation begins within the ceramic at the metallization–ceramic interface. Plastic deformation of the metal leads to accumulated stresses at the metallization edge [25]. When these stresses exceed the ceramic fracture toughness, cracks are initiated such as those seen in Fig. 1.

One method to increase time-to-failure due to delamination or crack formation is the substitution of Cu with Al as the metallization. The yield stress of Al is considerably lower than that of Cu (20 MPa and 70 MPa respectively) [25]. This reduces the mechanical stress in the substrate and improves overall lifetime. On the other hand replacing Al with Cu can introduce a new set of failure mechanisms. For example high strain levels in the Al can lead to cracks in the Ni metallization layer [25]. Additionally, the formation of hillocks in the Al layer [26–29] can occur under thermal and power cycling conditions, reducing the die attach fatigue life.

Table 1
Room temperature properties of Al_2O_3, AlN, and Si_3N_4 [22].

	Al_2O_3	AlN	Si_3N_4
Thermal cond. (W/mK)	26–35	150–180	20–30
CTE (ppm)	6.8–9	4.3–6.2	2.6–3.6
Flexural strength (MPa)	300–400	300–350	500–800
Dielectric strength (kV/mm)	10–20	14–17	10–14

Fig. 1. Conchoidal cracking in DBC ceramic [14]. Crack is initiated at the copper edge and propagates within Al_2O_3.

Substrate failure due to delamination and cracking is induced by thermomechanical mismatch stresses at the edge of the metallization. That occur when the entire substrate undergoes a change in temperature, such as homogeneous heating in the process of reaching a steady state thermal condition. Thermal cycling is the chosen test method for analysis and acceleration of this failure mechanism. In contrast, the hillock formation associated with Al metallization is not limited to the metallization edges. Thermal cycling will accelerate this failure mechanism throughout the substrate while power cycling will lead to hillock formation close to the die attach.

2.2. Wirebond failure

Flexural failure and shear failure are the two dominant failure modes for wirebonds. Cyclic thermal loads coupled with the CTE mismatch between the wire, the power device and the power module package induce significant stresses on the interfaces and the wire itself [14].

Wire flexural fatigue is typically found in cyclic thermal profiles with relatively long cycle periods. This type of thermal profile results in heel cracking of the wirebond and can be assessed through long dwell time power cycling or thermal cycling of the power module.

Shorter thermal cycles typically result in shear fatigue of the wirebond. This failure mode is often observed as wirebond liftoff or shearing. Unlike flexural fatigue, the shorter thermal cycles result in localized thermal mismatch and can thus be assessed by shorter duration power cycling.

It has been shown that Cu, as a substitute for Al wirebond material, considerably improves lifetime [17,30]. A multitude of factors contribute to this improved reliability of Cu wirebonds. For example, the electrical and thermal conductivity of Cu is approximately 40% higher compared to that of Al reducing conduction losses, temperature gradients and absolute temperatures. In combination with the lower CTE mismatch to Si and to the power substrate, reduced thermal strains in the wirebond are exhibited at the wirebond-metallization interface. Lastly, Cu is stiffer, more creep resistant, and possesses a higher yield strength, reducing inelastic strain damage during fatigue.

2.3. Die attach and baseplate attach fatigue

Conventionally, solders have been applied as die-to-substrate and substrate-to-baseplate interconnect material. They possess low melting temperatures, low strength and exhibit a high creep tendency at elevated temperatures limiting their fatigue life. The reliability of these solders are traditionally assessed by low frequency thermal cycling with homogeneous temperature

Please cite this article in press as: Squiller D et al. Physics-of-failure assessment methodology for power electronic systems. Microelectron Reliab (2014), http://dx.doi.org/10.1016/j.microrel.2014.07.123

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