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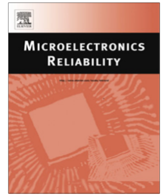

Influence of dicing damages on the thermo-mechanical reliability of bare-chip assemblies

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ABSTRACT

Increased demands for the integration density of electronics initiate a turnaround in packaging technologies, away from packaged constructions towards bare-chip-assemblies. A particular challenge of using bare-chips is the avoidance of chip fracture during processing and subsequent use. In this study a comprehensive portfolio of methods to predict the risk of chip fracture for bare-chips is shown. The basis is an investigation on the influences of different dicing techniques on the breaking strength of silicon chips. The stress resistivity of the chips shows huge differences, for instance 110 MPa after diamond-scribing up to 1473 MPa after thermal-laser-separation. Additionally, damages induced by the dicing were studied using scanning electron microscopy. The analysis of the size effect of diced silicon chips enabled to calculate the scaling parameter which is a size and stress independent strength value. All obtained results were used to develop a probabilistic reliability model for bare-chip-assemblies which describes the risk of chip fracture during the die attachment.

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1. Introduction

The use of bare-chip-assemblies has become a common concept of the assembly and packaging technology. Compared with packaging techniques using encapsulated chips, these packages offer higher integration densities and lower costs. However, the thermo-mechanical stress on the bare chips is crucial, both during assembly and packaging processes and during use in a device. Hence, chip fracture is an important failure mechanism of those technologies. In order to avoid chip fracture, the reduction of stresses was in the focus of research during the last years. This can be achieved by an exact matching of the important material parameters, e.g., the Coefficient of Thermal Expansion (CTE) [1]. For many bare-chip-assemblies proper matching is impossible, because substrates are often determined by other functionalities. For instance in power electronics an electrical connection of the chip backside to the substrate is needed (Fig. 1). Thus, chip fracture in case of bare-chip-assemblies is still an unresolved problem (Fig. 2) [2,3].

Chip fracture occurs, if the stress exceeds the breaking strength. Thus, chip fracture can be avoided by increasing the chips breaking strength. In some publications, the strong influence of the used dicing technology on the breaking strength of chips, due to flaws and micro-cracks, is shown [5]. To describe the phenomena of chip fracture, a fracture model is needed, which includes both, the stresses as well as the breaking strength of the chips.

In this investigation such a model has been developed. For this purpose, the influence of different dicing technologies on the breaking strength was investigated. Chips were diced by means of diamond-scribing, blade-dicing, stealth-dicing, water-jet-laser-dicing, deep-reactive-ion-etching and thermal-laser-separation. The damages caused by dicing were analyzed by means of optical and scanning electron microscopy. Based on the breaking strength measurements, an analysis of the chip size effect and the die attachment stresses were performed, and a mathematical formalism to describe chip fracture was developed.

2. Dicing technologies, specimens and methods to measure the breaking strength

2.1. Samples to compare dicing technologies

Today many different dicing techniques are available, based on mechanical, thermal or chemical principles. For instance Fig. 3 shows schematically the used laser based dicing technologies. For stealth-dicing a laser with a wave length of 1090 nm is used. Silicon is transparent for this laser, but the light beam is focused on the middle of the wafer thickness. In the focus point the photon density is high enough for non-linear absorption. Due to controlled absorption in the focus point the silicon is melted and recrystallized. With

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Fig. 1. Typical power module with an IGBT and two diodes connected as a half-bridge circuit [4].

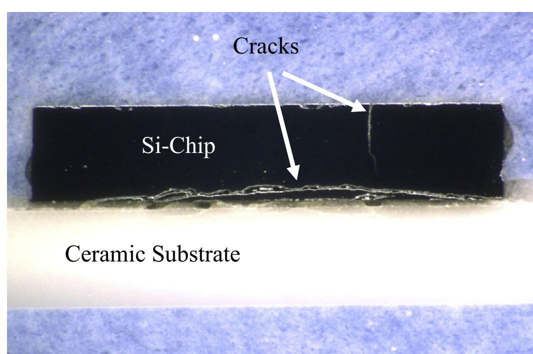

Fig. 2. Chip fractured after the mounting process with a vertical and a horizontal crack.

the laser a line of recrystallized Silicon is induced at predetermined breaking points, the SD-Layers. The wafer then is separated in to the chips along these SD-Layers by tensile stresses. Much different are the water-jet-laser-dicing and the thermal laser separation. The water-jet-guided laser uses the cooling water jet as a waveguide for the laser beam, the laser then operates like an ablation laser. In addition to the laser based techniques samples were prepared with blade-dicing, diamond-scribing and plasma-dicing. The different techniques cause different types of damages and in consequence the breaking strength of a chip strongly depends on them.

Modern dicing machines offer many options to optimize the process. In this investigation the actual state of dicing in industrial chip manufacturing was in the focus and thus, all samples were diced by industrial or institutional partners, which have a routine in dicing, using their dicing machines and parameters. In order to achieve a maximum of comparability for all samples, independent on the dicing technique, the same standard prime-double-side polished 4″-Wafer with a nominal thickness of 525 μm was used. To compare the breaking strength after the dicing, silicon strips with a size of 20 mm × 4 mm were cut out of the wafer and tested by means of 4-point-bending test.

2.2. Specimens to analyze the size effect

The size effect describes the phenomenon of different breaking strengths depending on the size of the measured component. The smaller the component the higher is the measurable breaking strength and vice versa. It was first specified in the case of tensile bars by Weibull [6]. The basic idea is that all material fracturing is initialized by a micro crack or void. It is assumed that micro cracks are a priori present in a material and under load they can start growing which leads in total fracture. A growing crack is called critical. Whether a crack is critical or not depends on the size of the crack and the stresses near the crack. The size effect is a statistical effect which describes the risk of having a critical crack in a material, the bigger the sample the higher the risk of having a large and critical crack in the material. With respect to the size effect, the breaking strength of a chip depends on the stress profile across the specimen which is applied for the measurements. Correspondingly, the risk of fracture in an application is also determined by the chip size and by the profile of the stresses which act on the chip in an application. Thus, the size effect is an important part to modeling the failure due to chip fracture.

To investigate the size effect of silicon chips, the breaking strength of samples with different sizes were measured. The samples had different lengths and widths. The length was varied from of 0.6 mm to 20 mm, while the width was diversified in the range of 0.3–4 mm. For this investigation the chips were diced by blade-dicing. The samples were again prepared out of the standard prime-double-side polished 4″-Wafer. All samples were diced with the same machine (Disco DAD321), the same blade (HEDD2050) and parameters (30.000 rpm spindle speed and 50 mm/s feed speed). The strength tests were done using three-point-bending. For each size 31 samples were tested and statistically evaluated with the Weibull distribution.

2.3. Breaking strength measurement

The three- and four-point bending tests are common methods to measure the fracture strength of brittle materials. As shown in Fig. 4, in both setups the sample is placed on two parallel supporter rollers. The mechanical load is applied by other rollers on the upper side of the sample. In case of three-point-bending, only one loading roller is used which is placed in the central position. In the four-point-bending, two loading rollers are used. Here, the distance between the lower rollers and the upper loading rollers is a quarter of the distance which the supporter rollers have.

During bending the top surface is in a compressive stress state, whereas the bottom surface is in a tensile stress state. As visible in Fig. 4, the tensile stress profile at the bottom surface in three- and four-point-bending is not the same. At three-point-bending, the stress increases linearly from the first supporter roller to the loading roller and decreases linearly from the loading roller to the second support roller. At four-point-bending, there are three different stress regions. The first region between the first support roller and the first loading roller is characterized by a linear stress ramp,

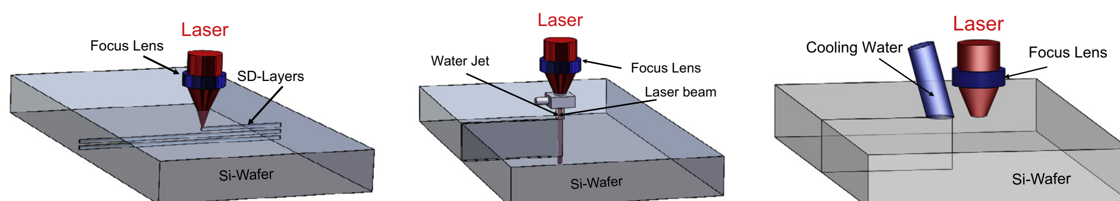

Fig. 3. Schematic of laser based dicing technologies: stealth-dicing (*l*), water-jet-guided-laser-dicing (*m*) and thermal-laser-separation (*r*).

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