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Degradation behavior in upstream/downstream via test structures

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ABSTRACT

The miniaturization process of CMOS components creates new challenges for the development of integrated circuits. Especially the connections with a tungsten via between two metal layers can be a problem. Changes in geometry can bear on reliability problems. For a robust metallization design it is necessary to know, how strong the influence of the tungsten via alignment affects the physical behavior. The lifetime of up- and downstream test structures with different overlaps as well as strong misalignment was determined by measurements. Investigations have shown that the alignments have a noticeable effect on the reliability and performance of test structures. The downstream line shows the expected lifetime behavior. For the upstream line no influence of the misalignment on the lifetime was found. Simulations are taken into account to understand the thermal–electrical and mechanical behavior.

1. Introduction

Due to the miniaturization process the metallization system is still one of the major problems in integrated circuits. Based on the increased complexity it is a challenge, that has to be accepted. To avoid time consuming long term stress tests the electromigration (EM) reliability of metallization systems is determined by temperature and current accelerated stress test. To get the information about the different failure mechanisms in normally standard electromigration tests, vias with different overlaps are used [1]. Typically if a higher applied current is necessary the number of vias is raised, but this is leading to a consumption of more chip area. Also the design of the via overlap comes into the focus of interest. A wider overlap does not improve the lifetime. In [2] is shown that a wrong overlap size for tungsten vias leads to a reduced lifetime. Very small overlaps are acceptable for digital applications. For higher DC stress and higher thermal load some thumb roles are necessary to use the most suitable line-via-combination. In addition the influence of via arrangement plays an important role [3,4]. Furthermore it has been found that an optimal overlap area for tungsten vias exists. In [2] a determination of the via overlap width for best lifetime performance for a downstream AlCu metallization with tungsten plug is shown. A variation of the dimensions of the overlap size was done without any misalignment. Measurements and simulations were in good agreement and showed an optimal overlap of 0.3 μm near the minimum design rule.

This work completes the investigations concerning the influence of the overlap design on the electromigration behavior. The influence of the overlap size of an upstream test structure as well as a misalignment of the tungsten via in up- and downstream test structure is presented here. In the downstream structures of [2] the wide metal layer is in metallization 2 (M2) in the upstream structures the wide metal layer is in metallization 1 (M1). In Fig. 1 a SEM (scanning electron microscope) picture of the upstream via structure is shown.

2. Model and simulation process description

Apart from measurements a 3D finite element model of an upstream and downstream structure was built. The simulations should help to understand the thermo-mechanical and thermal–electrical behavior under harsh test conditions. In Fig. 2 the mesh of the 3D finite element model of an upstream structure without covering dielectric for a better overview is shown. Not only the metal line was simulated also the covering liners, dielectric and the silicon substrate were considered in the 3D model. The simulations are carried out with ANSYS®. The element 'birth and die' capability can be used to determine the process induced stress [5]. The procedure is described in [6]. Out of this the pre-stress due to the specific temperatures of every single process step is calculated for the whole metallization system. In addition the mass flux divergence due to electromigration (EM) was calculated with

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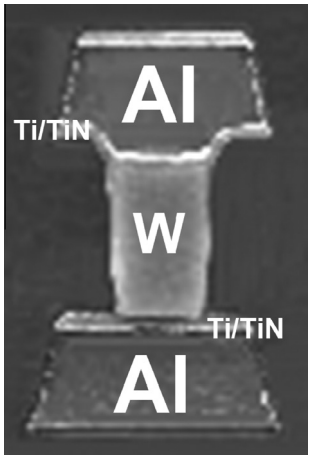

Fig. 1. SEM (scanning electron microscope) picture of the via structure.

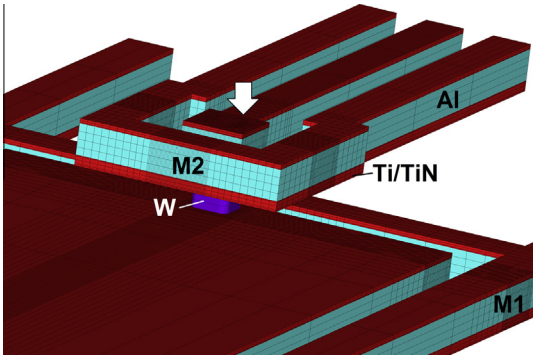

Fig. 2. Mesh picture of 3D finite element model of an upstream structure without covering dielectric (red = Ti/TiN liner, purple = tungsten via, cyan = Al). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

a user-routine by using the thermo-mechanical and thermal–electrical results of the finite element analysis of ANSYS® [7]. The thermomigration can be neglected [8]. With the help of this type of analysis it is possible to determine the weakest part inside a structure as well as to carry out a comparison between different metallization structures. The simplified mathematical description of the mass flux J_{EM} and the mass flux divergence div J_{EM} is shown in Eqs. (1) and (2):

$$\vec{J}_{EM} = \frac{N}{k_B T} eZ^* \vec{j} \rho D_0 \exp\left(-\frac{E_A}{k_B T}\right) \quad (1)$$

$$\mathrm{div}\left(\vec{J}_{EM}\right) = \left(\frac{E_A}{k_B T^2} + \frac{\alpha_T \rho_0}{\rho} - \frac{1}{T}\right) \cdot \vec{J}_{EM} \cdot grad(T) \quad (2)$$

In these equations N is the atomic concentration, eZ^* the effective charge of an ion, j the local current density, ρ the specific resistivity α_T is the temperature coefficient and D_0 is the self-diffusion coefficient. E_A is the activation energy, k_B the Boltzmann constant and T the local temperature. In these calculations a mass flux due to concentration gradients was not considered. In the case of a positive mass flux divergence the location can be regarded as a possible region for a void formation and a negative value as a possible region for hillock growth. A hillock growth was not investigated.

The mechanical and electrical material parameters of the metallization system used in the investigations are given for a temperature of 300 K in Table 1. The thermal conductivities are given in Table 2 and the material parameters for the calculation of the mass flux and mass flux divergence are given in Table 3.

Table 1
Material properties of the metallization system (T = 300 K).

Material	ρ (μΩcm)	α (10^{-6}/K)	E (GPa)	ν
Al	3.16	23.2	68.90	0.340
SiO_2	10^{18}	0.498	64.72	0.160
Si	4.4×10^6	2.64	98.7	0.450
Ti	47.8	8.30	110	0.360
TiN	2.00×10^2	9.35	80.60	0.208

Table 2
Thermal conductivity.

Material	300 K	400 K	500 K	600 K
Al	2.37	2.40	2.37	2.32
SiO_2	0.0138	0.0151	0.0162	0.0175
Si	1.480	0.990	0.762	0.619
Ti	0.208	0.199	0.191	0.183
TiN	0.230	0.241	0.252	0.261

Table 3
Physical properties for aluminium.

Physical properties	Value
Z^*	−10
k_B	1.38×10^{-23} J/K
E_A	0.7 eV
D_0	1.71 cm^2/s

3. Test and simulation results for the overlap variation

Standard electromigration accelerated tests were carried out for the different test structures with different overlap. The test temperature was set to 240 °C and the applied current was set to 15 mA. In Figs. 3 and 4 the lifetime of a via up- and downstream overlap variation is shown. The highest lifetime downstream was found for an overlap of nearly 0.3 μm.

Top metal structures showed comparable effects like the downstream structures but the optimum was not as clearly distinct as for the downstream structure.

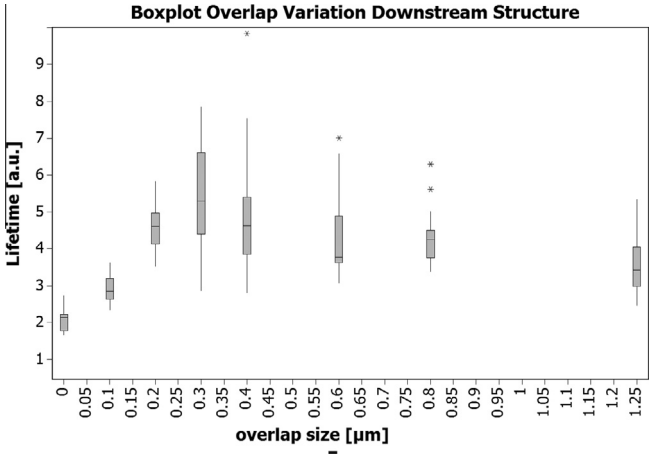

Fig. 3. Lifetime in a.u. of an downstream via overlap variation.