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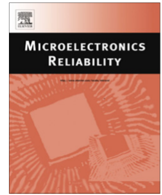

Focused ion beam contact to non-volatile memory cells

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ABSTRACT

Electrical characterization of non-volatile memory cells has been performed. A focused ion beam (FIB) contact procedure is presented that allows to contact the floating gate.

Calculations and measurement results on an exemplary floating gate memory cell show intact cell structure with limited retention time after FIB modification. The presented procedure allows the measurement and control of the previously unavailable floating gate current and voltage.

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1. Introduction and background

Non-volatile memories (NVM) are a fixed component for very many integrated circuits (IC). They allow for a flexible product design and possible post-manufacturing modification to parts of the design. Program code, calibration data or customization parameters are typically stored in NVM. Often, the amount of required storage is small and would not justify the use of expensive two poly layer silicon processes. Instead, standard complementary metal oxide semiconductor (CMOS) devices are used to achieve NVM functionality with only a single poly layer.

A floating gate (FG) is fabricated that connects a MOS capacitor to a transistor using only gate layer drawing (e.g. poly silicon). The transfer function between the bulk terminal of the capacitor and the drain and source terminals of the transistor exhibits a shift in voltage depending on the amount of charge stored on the FG. Reading such a NVM cell (transistor) is conducted by applying a fixed bias and measuring the drain current. Altering the charge on the FG is performed by various methods, including Fowler–Nordheim tunneling [1] (FN), hot carrier injection [2] (HCI) or channel initiated secondary electron injection [3] (CISEI). Typical implementations connect multiple of those transistors to form an array for storing multiple bits of information.

Conventional failure analysis (FA) for NVM circuits is limited to accessing the normal cell terminals. This allows to measure the cell in its normal operation. Identifying failures in connection with the gate oxide of the transistor or capacitor is not always possible since the floating gate can not be accessed. Using a focused ion beam (FIB) tool, opening the floating gate and depositing a conductor is possible from pure mechanical point of view. By the work with a charged particle beam, static charge could build up anywhere on the device leading to unexpected static discharges that may result in damage to the FG. As it is often the case in failure analysis (FA), only very few devices are available for analysis, making success a must.

This work shows exemplary approaches to such difficult situations with success and failures just alike. During the work, many FG devices were modified in a FIB process and subsequently analyzed using standard electrical FA methods.

2. Focused ion beam contacting

NVM devices may be analyzed electrically without difficulty up to a certain level of accuracy. For example, by using a probing station, all standard connections of a single NVM cell (excluding the FG) are connected to a parameter analyzer and subsequently biased and measured electrically. For such connections, a FIB is used to directly approach only those nodes that the analysis requires. As the cell terminals are connected to a large number of other nodes with low resistive paths to ground, charging is not critical during the use of the charged particle beam. Note that the FG is not contacted by such a standard work-flow. If additional accuracy is desired, contacting the FG is possible. The use of a charged particle beam when closely approaching the FG is a dangerous situation for ESD damages. Thus, careful planing of the sample preparation and FIB CE steps is required.

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The small outline (SO) package of the samples of this work were opened chemically using a jet-etch system to remove the package material. Ideally, bondwires and device surface are kept intact without modifications during the decapsulation. At this stage, the passivation layer was exposed for further steps.

A standard FIB CE procedure could now be rolled out to open the FG layer, deposit conducting material (see Fig. 1) and subsequently use this contact to measure the FG. Still, such a naive approach would be unlikely to succeed as the FG conducts the full beam current (see 3 in Fig. 1). For an improved success rate, the process parameters should be optimized prior to starting the CE procedure. The optimization could be carried out using a number of different conditions. In this work, we show how the standard operating conditions of the NVM are used to derive a desired sample current. Furthermore we estimate the sample current from different measurements on the FIB system. Using these information, a desired beam current and subsequently FIB box operation parameters are derived for contacting the FG (see 2 in Fig. 1). Successful approach to the FG was accomplished and subsequently the characteristic of the gate could be measured electrically.

2.1. Stress budget estimation

To minimize the influence of preparation procedure, the stress budget available for a single memory cell was estimated based on production parameters of the FG technology. For a given minimum number of write cycles N specified by the technology and the capacitance C_{FG} of the FG and the nominal threshold voltage shift ΔV_{TH}, the amount of charge Q_{max} transferred during the designed lifetime of a single cell is calculated by

$$Q_{max} = N \Delta V_{TH} C_{FG} \quad (1)$$

For the device used, the maximum designed charge transfer is estimated as 58 nC. After the maximum number of write cycles, the manufacturer specifies the percentage of fully functional ICs with p, typically containing 3σ. As the minimum number of write cycles is given per device and not per cell, the probability p_f for failure after N write cycles for a single cell is calculated from the device failure probability p by

$$p_f = 1 - \sqrt[N]{p} \quad (2)$$

For a 8 kb large array of cells and designed endurance of 3σ, this expression gives $p_f \approx 3 \times 10^{-8}$, making it very unlikely for a single cell to fail after the maximum number of write cycles.

2.2. FIB stress estimation

The FIB charged particle stress on the device is estimated from measurements on the DCG Systems OptiFIB. When the FG is opened by the FIB, the ion beam targets silicon material and stress is estimated by measuring the sample current as shown in Fig. 2. The influence of the charged particle beam on the device is, in this case, dominated by the introduced sample current. To estimate the stress imposed on the FG during the contact procedure, the sample current was measured for different beam currents when targeting silicon material [4], see Fig. 2. The sample current is linearly connected to the beam current with a factor of 2,6 for the 30 keV Ga^+ beam on silicon.

Furthermore, before contacting the FG, the beam charges up the insulating surface of the device. Measuring the sample current on insulators is difficult using conventional technique. Instead, a specialized charge sensor was used to estimate the charge introduced onto the device surface from the charged particles [5]. The charge sensor is capable of measuring the amount of charge deposited onto the sample surface during ion beam irradiation with high precision. To ease the interpretation, the amount of charge present on the surface was measured before and after a single raster scan of the ion beam, see Fig. 3. Using the beam and scan parameters, the sample current for insulating targets was derived:

$$I_{sample,ins} = \Delta Q_{sensor} \frac{A_{scan}}{A_{box}} \frac{1}{t_{frame}} \quad (3)$$

The current on insulating samples was estimated as initially 62,3 pA (1 in Fig. 3) and decaying to 28,6 pA (2 in Fig. 3) for a 20 pA beam current. These results suggest, that during removal of the insulator above the FG, the influence on the FG is static only, whereas it will be higher during the actual contact procedure.

For full stress estimation of sample preparation, the etching and deposition speeds should be derived. For example, using a 100 pA ion beam on a 3 µm × 3 µm box area, the etching speed was measured to be 99 s/µm [4]. With the etching speed, the full procedure is planned in detail and subsequently the stress budget may be met by modifying the FG contact procedure accordingly. Additional information on the deposition speed helps to reduce the FIB work steps but is not necessary for minimizing sample stress.

2.3. Deriving FIB preparation parameters

Using the FIB parameters, a preparation procedure is designed that meets the stress budget of the cell. The FIB FG contact procedure consists of the two goals of opening and subsequently contacting the FG. In order to allow needle probing on the FG, the resulting contact should support a maximal mechanical stability and minimum resistive connection to the FG. As the FG does not require high currents, the connection resistance is of lesser importance. Even tunneling currents – the highest currents occurring at the FG – are very low, a resistance of even hundreds of kilo ohms does not play a significant role.

Thus, the steps taken in this approach are: (1) Open, connect and deposit conductor for all terminals except the FG. (2) Deposit

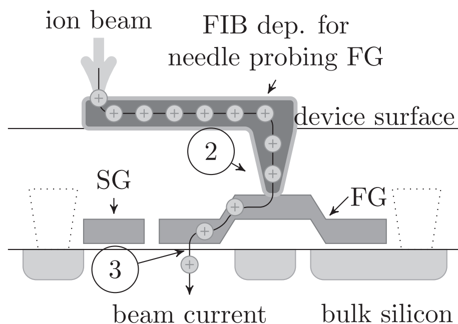

Fig. 1. Schematic view on FIB CE for EEPROM cells with floating gate (FG) and select gate (SG) and involved stress to gate oxide. Contacts to drain/source/control gate indicated by dotted lines.

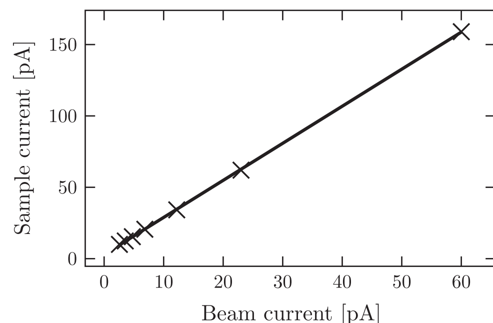

Fig. 2. Device current of 30 keV Ga^+ ion beam on silicon with least mean square fit ($m = 2,6, y_0 = 2.66$ pA).

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