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Impact of gate drive voltage on avalanche robustness of trench IGBTs

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ABSTRACT

In this paper, the impact of the gate drive voltage on avalanche capability of Trench-IGBTs is deeply analyzed by means of infrared (IR) thermal measurements and TCAD simulations during Unclamped Inductive Switching (UIS) test. The reported results are carried out for a case study on a 1.2 kV – 200 A rated device. Experimental results show the effect of the gate drive voltage during avalanche operation. A possible non-uniform current conduction for unipolar gate-driver case is proven using transient thermal maps. As a consequence, the dependence of the actual breakdown voltage (V_{BR}) of the device active area with a negative gate biasing is investigated for trench structures. A reduction of the V_{BR} and a slighter interplay between the T-IGBT cells and the termination area is demonstrated for a negative gate bias during the blocking state using ad-hoc TCAD electro-thermal simulations. Finally, the boosted avalanche capability is proven for under-biased case and a theoretical explanation of the involved phenomena is provided.

1. Introduction

In recent years, many studies have been carried out to assess the avalanche robustness of new IGBT designs [1–4]. Experimental evidences and numerical simulations have pointed the attention toward the shape of the forward blocking *I–V* curve [5–8]. Particularly, the presence of a Negative Differential Resistance (NDR) branch has been demonstrated to be responsible of non-uniform current conduction and a reduced avalanche energy capability. For Trench-IGBTs (T-IGBTs), however, the blocking characteristic is related to the gate potential also. It has been proved in a previous work [9] that a negative voltage applied to the gate terminal leads to a reduction in the V_{BR} and therefore the breakdown capability of the device is degraded. Additionally, in recent literature are present papers focused on the interaction between the device active region and the termination region during avalanche breakdown [10,11]. The reported results address the V_{CE} sudden decrease or time-oscillation with avalanche current path switching from the active region to the termination region [12]. It is also commonly accepted that for an avalanche rugged device, the interaction between termination and active area is crucial.

Besides these implications, nowadays the impact of a negative bias during blocking-state on the device avalanche robustness is not proven yet. Power devices manufacturers recommend the use of negative gate voltage (bipolar driver) to safely turn-off and block IGBT modules. However, in areas with nominal currents less than 100 A the negative gate voltage is often omitted for cost reasons (unipolar driver) [13]. When switching to 0 V two effects may come into play as showed in Fig. 1: (i) parasitic turn-on via the Miller capacitance (ii) parasitic turn-on via stray inductances.

The general practice is to provide a negative gate bias of −15 V. This ensures adequate turn-off for the application and to negate the effect of Miller induced current in a bridge configuration if a high *dv/dt* is applied to the devices. In the standard bipolar gate-drive circuits the gate-emitter voltage swings from −15 V to 15 V during the switching transition.

In view of these considerations and since the design of a T-IGBT that accounts for an avalanche rugged device introduces a severe trade-off with the on-state performances [14], the investigation of possible effects of the gate-drive voltage also on the UIS capability becomes of a paramount importance. To the purpose, in the present work, a case study is conducted on a 1.2 kV – 200 A rated T-IGBT with both experiments and simulations approaches.

2. Experimental analysis of UIS behavior

The Device Under Test (DUT) avalanche behavior has been fully characterized by means of a UIS tester machine [15]. The load

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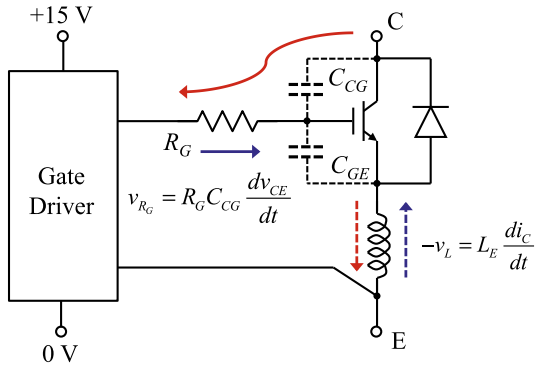

Fig. 1. Current via the Miller capacitance of the upper IGBT (continues arrows) and induced voltage across the emitter inductance (dashed arrows).

inductor value is chosen to be 10 mH to give reasonable trade-off between the electrical and the thermal stress across the DUT [10]. The DC voltage, used to charge the inductor, has been changed up to a maximum value of 180 V, to achieve different desired peak currents. The gate driver circuit was based on a SCALE™ Concept 2SD315AI power driver. Concept 2SD315AI drivers can provide very high output currents (±15 A in bipolar-mode with ±15 V) so they can be used in high-power applications up to 1.7 kV [16]. Two kinds of UIS tests have been performed: (i) with unipolar gate-voltage and (ii) with bipolar gate-voltage. In the first case, in the following referred as *Case "A"*, the driver circuit has been properly modified to operate in the positive range +15 V (ON state) – 0 V (OFF state). Fig. 2 shows the V_{CE} waveforms during UIS tests at different inductor currents.

The DUT exhibits saw-tooth type oscillations on the V_{CE} waveforms. This behavior is related to a non-uniform current conduction state, with possible hogging and filaments hopping phenomena [17,18]. In the second case, in the following *Case "B"*, the gate drive circuit operate with a bipolar voltage capability (+15 V/−15 V). The same experiments of the previous case have been repeated on the same device. Fig. 3 show the collector to emitter voltage waveforms for three different current levels.

In this case, the actual V_{BR} is lower, and the V_{CE} traces does not exhibit the previously observed oscillation behavior. To better investigate the aforementioned scenario, IR thermal measurements [17] have been also performed during the previous UIS experiments. Fig. 4a reports thermal maps at different time instants for a single UIS experiment (I_{peak} = 20 A) in Case "A". An uneven temperature (current) distribution on the device area is

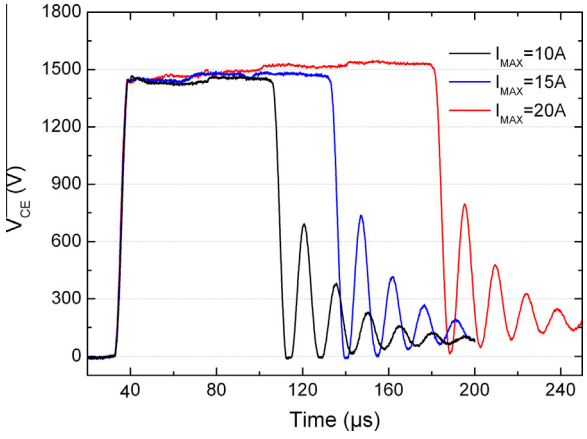

Fig. 2. V_{CE} waveforms during UIS tests (Case "A") at different inductor currents.

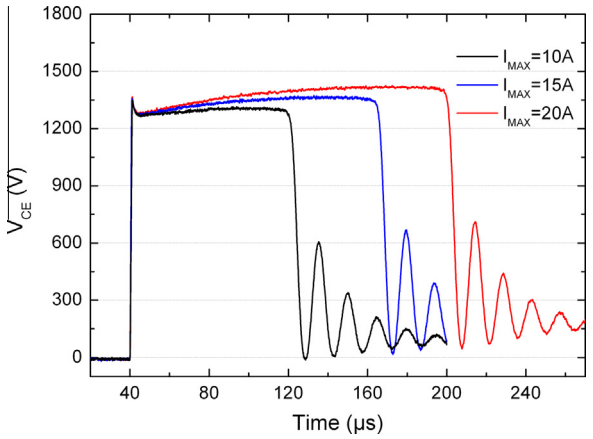

Fig. 3. V_{CE} waveforms during UIS tests (Case "B") at different peak currents.

identified. Moreover, temperature maps also indicate the presence of current conduction paths in the termination area. For the same UIS conditions, Fig. 4b report the transient thermal map evolution in the Case "B" experiment. It is evident that neither uneven temperature distribution is present nor current hogging.

The maximum avalanche energy E_{avMAX} has also been evaluated increasing the UIS peak current until the device fails. The results prove an $E_{avMAX} \approx 2\,J$ in the Case "A", in spite of about $4\,J$ for the Case "B". The above analysis clearly indicates a strong correlation between the gate bias voltage, during the off-state, and the device avalanche behavior.

3. TCAD simulations

To have a deeper insight into the involved phenomena, TCAD simulations have been performed. First, the effect of the gate biasing voltage on the T-IGBT single cell has been investigated. The results of a parametric simulation are depicted in Fig. 4. Besides a shift to left of the *I–V* blocking curve, it has been found that a negative gate voltage impacts on the NDR extension, with a lower current density at the transition point (TP) from NDR to Positive Differential Resistance (PDR). In Ref. [8] it has been assessed that non-uniform (or filamentary) current conduction is due to the presence of a NDR branch in the *I–V* avalanche curve, while the current density at TP point defines the filament area. Accordingly to these assertions, the results in Fig. 5 give a first indication on the benefit of a negative gate bias.

In Fig. 6 the static electrical field distributions for V_{GE} = 0 V and I_C = 15 A case is shown. As expected, for the trench structure, the highest electric field in the silicon region is located beside the trench around the trench corner. Nevertheless, a negative voltage was applied to the gate, although the depletion region in the p-base was narrowed due to accumulation of holes, the horizontal electric field in the n-base region besides the trench is larger due to the extra negative amount of potential applied to the gate. Consequently the total electric field in the n-base region around the trench corner increases.

Hence the Impact Ionization (II) around the trench corner increases and therefore the V_{BR} of the active area is reduced. Fig. 7 clearly indicate the increased II rate for negative gate bias. Since the V_{BR} of the termination region is not affected by the gate voltage, the interplay between active region and termination region can be affected by the gate bias.

Construing Fig. 8, it is possible to foresee that if the device is not under-biased (V_{GE} = 0 V), during the avalanche the current will initially flow entirely in the termination region due to a lower

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