Microelectronics Reliability xxx (2014) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Impact of active thermal management on power electronics design

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ARTICLE INFO

Article history:
Received 3 July 2014
Accepted 8 July 2014
Available online xxxx

Keywords:
Chip utilization
Active thermal management
Reliability

ABSTRACT

Power electronic system design is typically constrained by the thermal limitation so by the overall losses and the peak current. To stay within the maximum current, reached only during transients, the system is typically overrated. Active thermal management is used to control the maximum temperature and the temperature swing to reduce failures that are mostly caused by them. In this paper it is proposed to use the active thermal management to reduce the switching losses or to move them to less stressed devices, during transients, such as a module can reach an higher current, without violating thermal constraints, and the need of overdesign can be reduced. Hence an optimal and cost effective design of power electronics system is achieved.

1. Introduction

PWM voltage source converters have become widely used in several applications like traction, automotive or the generation of renewable energies [1,2]. The design of the system has to be cost effective, guaranteeing reliability at the same time. However, overdesign is a common practice to reduce failures, especially during transients, avoiding too high temperatures or excessive thermal swings.

This work proposes the use of a thermal management system not only for reducing failures related to overtemperature or temperature swings [3], but also for achieving a loss reduction in transient conditions to enable a better utilization of the existing hardware.

First, this work analytically analyzes thermal cycling of the junction temperature in an inverter and highlights how different operating conditions constrain the junction temperature. Practical examples how the thermal management system can control the losses with a benchmark of the possible stress reduction are given in Section 4. Conclusions for system design with thermal management are given in Section 5 and the results are summarized in Section 6.

2. Thermal models of power electronic modules

During operation, the power semiconductors cause losses P_{loss}, which are mainly generated by switching losses P_{sw} and conduction losses P_{cond}.

$$P_{loss} = P_{SW} + P_{cond} \tag{1}$$

The losses cause heating of the devices, which affects the operation of the semiconductors. Thereby excessive temperatures, which are approximately 150 °C for silicon, lead to an increased failure rate. In general high temperatures in the range (20 °C–150 °C) increase the losses and reduce the lifetime, while thermal cycling affects aging of the semiconductors, also being the prevalent reason for failures [4]. The chip size and the power semiconductor heat transfer capability influence the heat dissipation, whereby a decrease of the chip area worsens the heat transfer capability. This can be expressed in an increase of the thermal resistance R_{th}. The thermal resistances define the correlation of a temperature difference and the corresponding losses P_{loss} between two points (e.g. junction to case $R_{th,jc}$). For stationary analysis, the averaged junction temperature $T_{j,av}$ can be expressed with

$$T_{j,av} = T_c + R_{th,jc} \cdot P_{loss} \tag{2}$$

For a more accurate calculation for the transient temperature T_{inv} in an inverter at the time t_{end}, the calculation has to be made for every single switching operation.

$$T_{inv}(t_{end}) = \sum_{k=1}^{k_{end}} (P_{loss,k} - P_{loss,k-1}) \cdot \sum_{i=1}^{n} R_{th,i} \left(1 - \exp\left(-\frac{t_{end} - t_{k-1}}{\tau_i}\right)\right) \tag{3}$$

In this equation, the losses in each switching position are expressed with $P_{loss,k}$ and the switching frequency with f_s [5]. The parameter $R_{th,i}$ and τ_i are the datasheet values of the Foster thermal network. Using these datasheet values does not necessarily lead to

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http://dx.doi.org/10.1016/j.microrel.2014.07.069
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the precise junction temperature, because of parameter variations that result from the production process and aging effects [6]. However, these values obtain a safety margin to prevent overheating introduced by the manufacturer.

The times t_k represent switching times and can generally be expressed with (4) and (5), whereas $\Theta(k)$ depends on the modulation scheme and k_{end} represents the sample of the last switch before t_{end}.

$$t_{2k-1} = \left(\frac{1-\Theta(k)}{2} + k - 1\right) T_s \tag{4}$$

$$t_{2k} = \left(\frac{1+\Theta(k)}{2} + k - 1\right) T_s \tag{5}$$

For optimized utilization of three phase voltage source inverter, the maximum linearity is exploited by using SVPWM (space vector modulation) with added 1/6 of the 3rd harmonic:

$$\Theta(k) = m \cdot \left(\cos\left(2\pi k \frac{f_0}{f_s} + \varphi\right) + \frac{1}{6}\cos\left(6\pi k \frac{f_0}{f_s} + 3\varphi\right)\right) \tag{6}$$

The losses of the power semiconductors have to be calculated for each switching state. For an IGBT, the switching losses $P_{sw,T}$ and the conduction losses $P_{cond,T}$ can be expressed with:

$$P_{sw,T}(k) = f_s(E_{on} + E_{off}) \cdot \frac{\hat{i} \cdot \cos\left(2\pi \cdot k \cdot \frac{f_0}{f_s} + \varphi\right)}{I_{ref}} \cdot \left(\frac{V_{out}}{V_{ref}}\right)^c \tag{7}$$

$$P_{cond,T}(k) = \left(\hat{i} \cdot \sin\left(2\pi \cdot k \cdot \frac{f_0}{f_s} + \varphi\right) \cdot u_{ce,sat} + r_{ce} \cdot \hat{i}^2 \cdot \sin^2\left(2\pi \cdot k \cdot \frac{f_0}{f_s} + \varphi\right)\right) \cdot \frac{t_k}{T_s} \tag{8}$$

In these equations, $\hat{i}$ is the magnitude of the current, E_{on} and E_{off} are the turn on/off losses at reference current and voltage, φ is the phase displacement of the current to the voltage, V_{out} is the voltage blocked by the semiconductor, V_{ref} and I_{ref} are the reference values for the measurement of the semiconductor losses and c is an empirical factor estimated to $c = 1.35$ [5]. The conduction losses of the IGBT are linearized with the constant voltage drop $u_{ce,sat}$ and the current magnitude dependent voltage drop r_{ce}. It needs to be mentioned, that the losses are only affected during the turn on time for positive voltage and positive current at the semiconductors. Similar to the IGBT, the losses for the diodes $P_{sw,D}$ and $P_{cond,D}$ can be expressed.

$$P_{sw,D}(k) = f_{sw} \cdot E_{rr} \cdot \left(\frac{\hat{i} \cdot \cos\left(2\pi \cdot k \cdot \frac{f_0}{f_s} + \varphi\right)}{I_{ref}}\right)^d \cdot \left(\frac{V_{out}}{V_{ref}}\right)^d \tag{9}$$

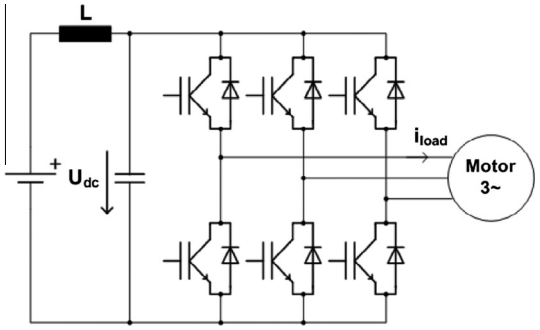

Fig. 1. Simplified drivetrain of an electrical vehicle.

$$P_{cond,D}(k) = \left(\hat{i} \cdot \sin\left(2\pi \cdot k \cdot \frac{f_0}{f_s} + \varphi\right) \cdot u_D + r_D \cdot \hat{i}^2 \cdot \sin^2\left(2\pi \cdot k \cdot \frac{f_0}{f_s} + \varphi\right)\right) \cdot \frac{t_{on,k}}{T_s} \tag{10}$$

The parameter d is an empirical factor for the losses and is set to $d = 0.6$, while u_D and r_D represent the linearization of the diode forward characteristics. Losses are only generated for positive voltages and negative currents.

For demonstration an electrical vehicle with a 2-level voltage source inverter fed by a battery system is chosen such as in Fig. 1. By applying (4) with a DC-link voltage $U_{dc} = 700$ V, the modulation scheme of (6), a phase displacement $\varphi = 0$ and a modulation factor $m = 1.16$, the maximum conduction time for the IGBT is chosen. The case temperature is set to $T_c = 80$ °C and an output current $\hat{i} = 25$ A is fed, which is similar to the rated DC current of the selected power module [7]. The fundamental frequency is $f_0 = 50$ Hz and the switching frequency is $f_s = 2.5$ kHz. Furthermore, the temperature calculated by using the average losses $T_{j,av}$, calculated with (2), is shown in the figure. It can be observed, that the thermal cycles obtain a magnitude of $\Delta T_{inv} = 15.5$ K. The temperature, which has been calculated by using the averaged losses, is within the thermal cycling of the precise calculation, but exceeds the average temperature.

3. Active thermal management

Since thermal cycling and high temperatures cause the aging of power electronic modules, the thermal swing has to be kept as small as possible. An approach to prevent excessive thermal cycling is to control the junction temperature in critical conditions [3]. A severe condition for inverters is to feed a variable speed

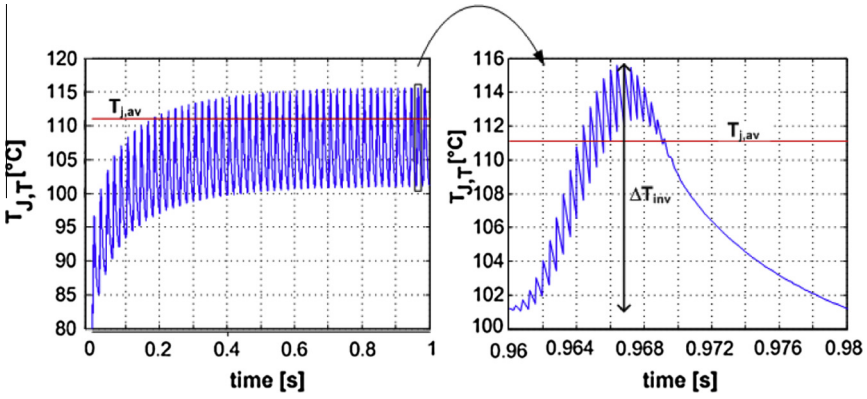

Fig. 2. Junction temperature of an IGBT in a PWM inverter ($\hat{i} = 25$ A, $U_{dc} = 700$ V, $f_{sw} = 2{,}5$ kH): exact calculation (blue) averaged loss calculation (red). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Please cite this article in press as: Andresen M, Liserre M. Impact of active thermal management on power electronics design. Microelectron Reliab (2014), http://dx.doi.org/10.1016/j.microrel.2014.07.069