

NBTI degradation in STI-based LDMOSFETs



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ARTICLE INFO

Article history:

Received 26 June 2014

Accepted 8 July 2014

Available online 30 July 2014

Keywords:

NBTI degradation

STI-based LDMOSFETs

HCI

MR-DCIV

ABSTRACT

NBTI degradation in STI-based LDMOSFETs has been investigated by multi-region DCIV spectroscopy (MR-DCIV), a non-destructive and sensitive method to probe the interface states on channel, accumulation and STI region. A unified MR-DCIV current model was proposed based on its independency to the forward bias and temperature. Under the same negative gate stress condition, MR-DCIV current degradation was compared for nLDMOSFET and pLDMOSFET. Much larger MR-DCIV current shift was observed at channel and accumulation region with thin gate oxide thickness, indicating interface states generation at related regions. Our results show that more significant degradation for multi-finger device was consistent with NBTI degradation mechanism. High voltage device design with thermal management consideration is of crucial importance to guaranteeing the device performance and reliability.

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1. Introduction

With the advantage of the process compatibility with the mainstream standard Complementary Metal Oxide Semiconductor (CMOS), with an insertion of shallow-trench-isolation (STI) region in LDMOS devices, STI-based laterally diffused metal oxide semiconductor field effect transistor (LDMOSFET), have become popular for their better tradeoff between breakdown voltage and performance [1]. Due to the capability of handling high voltage and high current levels, reliability of power devices is of prime importance, most of hot-carrier-injection (HCI) studies are focused on nLDMOSFETs rather than pLDMOSFETs [2–4]. However, in some design, pLDMOSFET can be a better option for significant circuit simplification, and has been more and more used in the smart power application. As we know, in pMOSFETs negative bias temperature instability (NBTI) has become the major reliability concern [5] due to interface states generation under relatively high temperature. The performance limited by operation temperature for high voltage devices has been studied before, but NBTI related degradation in high voltage devices was less reported. Up to now, several characterization techniques have been developed to monitor the interface states in LDMOSFETs. Because of the potential damage of multiple level charge pumping (MLCP) [6] and complexity of low-frequency $1/f$ noise measurement [7], recently, a non-destructive multi-region direct-current current–voltage (MR-DCIV) technique has been proposed [8] to probe the interface states all over the channel, accumulation and STI drift region in

LDMOSFETs. In this paper, using MR-DCIV method, we would report NBTI degradation in STI-based LDMOSFETs and compare the degradation behavior in n- and pLDMOSFETs. Our studies presented the multi-finger device enhanced degradation and its correlation with high temperature accelerated NBTI degradation.

2. Devices and MR-DCIV technique

The STI-based pLDMOSFET with cross section in Fig. 1 was fabricated by a 0.18 μm silicon-on-insulator (SOI) CMOS compatible bipolar-CMOS-DMOS(BCD) process. SOI wafers have a silicon layer thickness of 1.5 μm , a p-type resistivity 8–12 Ωcm and a buried-oxide (BOX) thickness of 1 μm . The wafers had various doses of implantation to achieve the dose control in p-well and n-drift regions for obtaining an optimum reduced surface field (RESURF) effect in order to maximize the breakdown voltage and on-resistance. The off-state breakdown voltage is above 60 V. The on-state breakdown voltage is in excess of 40 V up to $V_{\text{gs}} = -5$ V.

A typical MR-DCIV current obtained from a fresh pLDMOSFET was shown in Fig. 2. During the MR-DCIV measurement, the source/drain to substrate junction was forward biased (V_F), the substrate current I_{sub} was measured when gate voltage was swept from accumulation to slight inversion. Several distinct MR-DCIV current peaks were corresponding to the interface states at channel, accumulation and STI drift region, respectively [8]. The individual MR-DCIV current peak height was proportional to the interface state density at channel, accumulation and STI regions in pLDMOSFETs.

MR-DCIV current level is sensitive to the temperature (T) at constant source/drain–substrate junction forward bias (V_F). The

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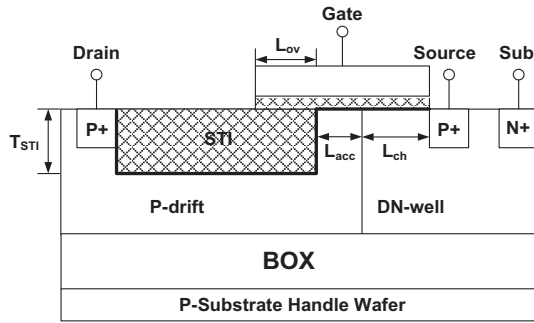


Fig. 1. A cross-sectional view of an STI-based pLDMOSFET.

relationship of extracted MR-DCIV current to V_F and T was obtained and summarized in Fig. 3. It was easy to find that the MR-DCIV current followed the Arrhenius law under various forward biases. With the increase of temperature from 25 °C to 150 °C, MR-DCIV current would change over several orders magnitude. And the parallel data for different forward bias also indicated the exponential dependence to V_F at a constant temperature. Over four orders of magnitude of MR-DCIV current, the good correlation with various temperatures and forward biases was modeled. The uniform MR-DCIV current can be expressed as

$$I_{\text{MR-DCIV}} = C \exp \left(23.3 V_F - 0.62 \frac{q}{K_B T} \right)$$

where the pre-coefficient C was a constant which was only proportional to the interface states density. Here the identical fresh device was characterized under various temperature and forward bias, the interface state density was assumed to be the same under various temperature and forward bias. This unified results suggested that the MR-DCIV current could be scaled accordingly for comparison at different temperature and V_F .

3. Results and discussion

3.1. Single finger device

In order to understand the NBTI degradation effect, constant gate voltage of -10 V at 125 °C was applied to nLDMOSFETs and pLDMOSFETs, respectively. Fig. 4 presented the evolution of MR-DCIV current after 5000 s NBTI stress. It was observed that after 5000 s NBTI stresses, MR-DCIV current at channel and accumulation region grew up for both nLDMOSFETs and pLDMOSFETs,

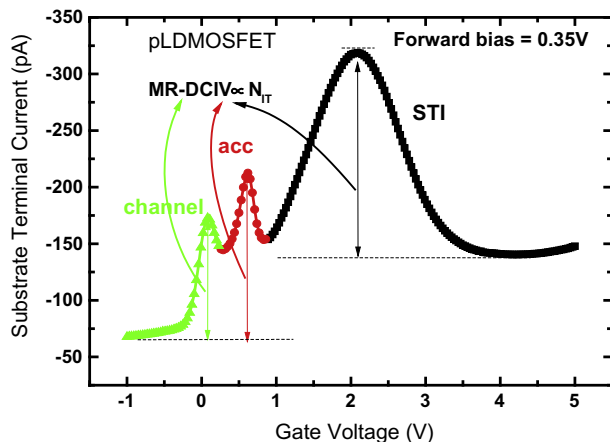


Fig. 2. A typical MR-DCIV current of fresh pLDMOSFET.

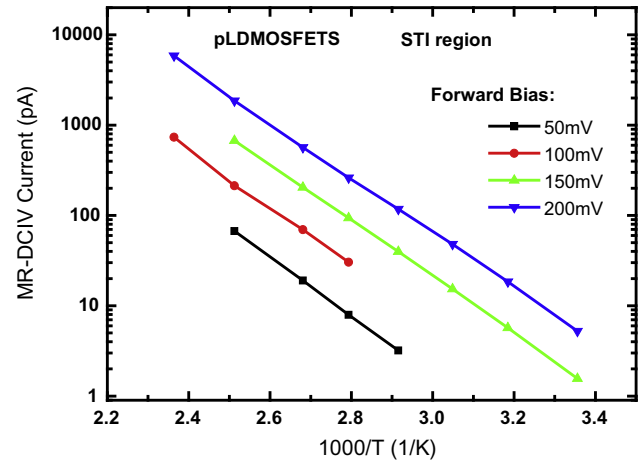


Fig. 3. MR-DCIV current at temperature from 25 °C to 150 °C.

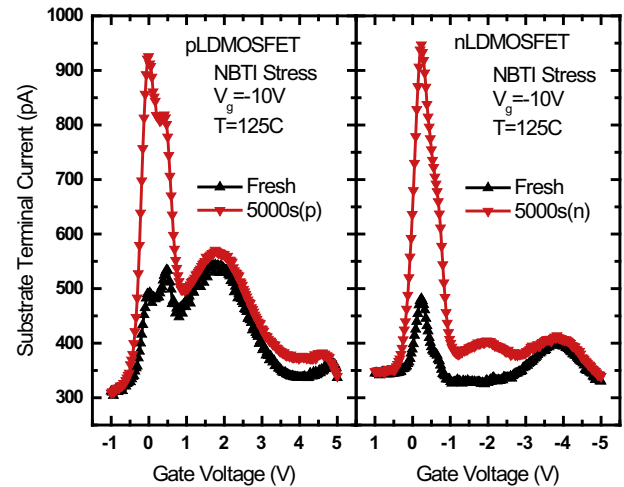


Fig. 4. MR-DCIV current degradation after 5000 s NBTI stress at pLDMOSFET (left) and nLDMOSFET (right).

indicating the interface states generation at channel and accumulation regions during NBTI stress. From Fig. 1, it was clear to see that the gate oxide was much thicker over drift region in LDMOSFETs, therefore the NBTI stress induced damages will mainly occur at channel and accumulation regions. The corresponding MR-DCIV current growth was observed. What is different from pMOSFETs dominant NBTI effect in CMOS technology, the degradation of MR-DCIV current after 5000 s NBTI stress was similar for both nLDMOSFET and pLDMOSFET in STI-based LDMOSFETs.

For pLDMOSFETs, the relative changes of MR-DCIV currents at channel and accumulation region were close to power-law time dependence, shown in Fig. 5, following the same NBTI degradation trend as standard CMOS devices [5]. Because the channel and accumulation region has an opposite doping type, which meant that the NBTI stress for pLDMOSFETs combined both normal NBTI stress for pMOS and nMOS device, the channel interface state generation rate was $2 \times$ larger than that of accumulation region.

On the other hand, the interface states generation was significantly increased with higher NBTI stress temperature. Due to the thinner gate oxide at channel region, the NBTI stress induced damages will be generated at channel region. Here, the MR-DCIV current normalized by channel component current peak is shown in Fig. 6 inset. In order to avoid the device-to-device variation, the relative change of interface state density at channel region

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