Brief paper

On the use of one bit quantizers in networked control[☆]

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ABSTRACT

This paper addresses the following problem in networked control: "If a control law is implemented over a channel that supports a certain fixed bit rate what is the best choice for the control update rate and, consequently, the number of bits carried in each sample?" A restricted architecture in which linear filters are used for the encoder/decoder is considered and a quantizer with linear feedback is deployed. Subject to these restrictions, a procedure for designing the controller and associated filters is presented. These filters are then deployed to choose the best number of bits per control update. It is shown, subject to the above restrictions, that it is generally best to use one bit per sample, in which case, the control update rate is equal to the bit rate. Our analysis has two points of departure from contemporary literature in this area. Firstly, we focus on bits per unit time, as opposed to bits per sample. Secondly we use a fixed number of bits in every time period as opposed to an average bit rate.

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1. Introduction

Control theory has traditionally ignored communication constraints, but the recent developments in networked control systems, and the problems arising there from, have inspired considerable interest in the interplay between communication and control (Antsaklis & Baillieul, 2004; Wong & Brockett, 1997). A major focus in this literature has been on the effect of network constraints on performance and stability; typical constraints are limits on (average) data rate, random delays and lost packets. There has been important progress in several areas, (see Braslavsky, Middleton, and Freudenberg (2007), Goodwin, Silva, and Quevedo (2010), Lian, Moyne, and Tilbury (2003), Ling and Lemmon (2004), Nair and Evans (2004), Nair, Fagnani, Zampieri, and Evans (2007), Nilsson (1998), Savkin (2006), Schenato, Sinopoli, Franceschetti, Poolla, and Sastry (2007), Seiler and Sengupta (2005) and Tatikonda and

Mitter (2004)). The current paper adopts an alternative point of view and assumes that the constraint is on the bit rate in the communication channel between control law and plant rather than the sampling rate. There are several ways that the question considered here could be formulated, for example where the constraint on bit rate lies between controller and plant, between plant and controller or both. Here, we explore the first of these options. This choice was motivated, in part, by the practical problem of inner loop power control in WCDMA mobile communications (Cea & Goodwin, 2011; Dahlman, Parkvall, Skold, & Beming, 2007). In this problem, the input update period is set to $\Delta = 0.667$ ms and, in traditional implementations, 1 bit per sample is used. However, it would be possible to maintain the same input bit rate whilst changing the input update period to $p\Delta$ and to use p bits/sample. This change of paradigm raises the question as to whether, or not, the choice $p = 1$, used in practice, is the best choice. Preliminary simulation studies conducted by the present authors suggest that 1 bit/update is actually the best choice. The bit rate is the product of the number of bits per sample and the control update frequency. Since p bits per sample permits 2^p quantization levels, a higher value for p reduces the quantization error but also increases the period over which the input must be held, therefore, the ability of the controller to reduce the effect of disturbances. This decomposition of the bit rate into the product of bits per sample and input update frequency results in an obvious trade-off and leads to the question: "What is the best allocation of a given bit rate into the
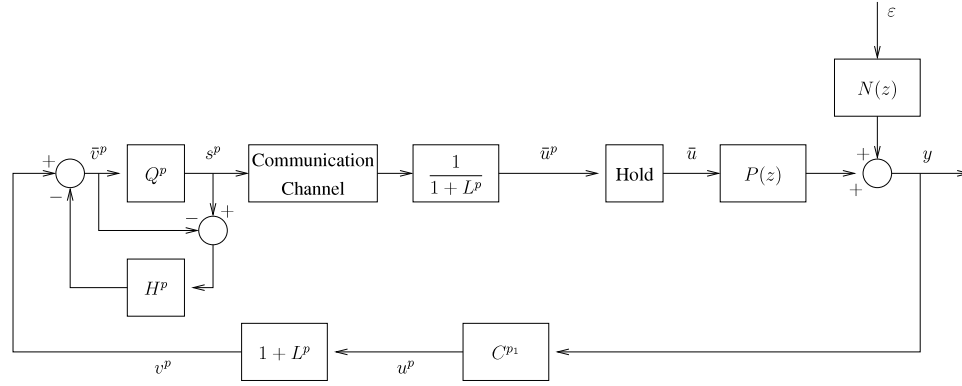
Fig. 1. Proposed four degree of freedom architecture (C^{p_1}, L^p, H^p and Q^p).

number of bits per sample and the number of control updates per second?" This paper addresses this question.

A restrictive (pragmatic) view of network control in which linear filters are utilized for the encoder/decoder pair is adopted. The single input single output case is considered, and a quantizer with linear feedback is deployed to assign the signal of interest to the available bits. The analysis is restricted to open loop stable systems. It would be interesting to relax these restrictions. However, these restrictions are used here to simplify the analysis. We leave it for future research to consider other scenarios. Subject to the above restrictions, a design procedure in which, for each choice of the number of bits in the quantizer, the optimal controller, encoder/decoder and quantizer feedback are chosen. These designs are then used to choose the optimal number of bits/control update. It is shown, surprisingly in our view, that one bit per control update is typically the best choice. Consequently a control update rate equal to the available bit rate is best. This choice corresponds to implementing the control law using a scaled sign function.

2. A class of models

Consider a single input single output linear continuous time system and assume the following:

A.1 The bit rate of the input channel (between controller and plant) is restricted to B_r bits/s so that $\Delta_1 = 1/B_r$ s is the smallest possible control update period.

The output is always sampled at period Δ_1 and an appropriate anti-aliasing filter is deployed at this sample period. Filtering at the lower sample period is implicit in the form of the controller. The input is held constant for p samples to allow a p bit quantizer to be used i.e. p bits are used to code the input signal. When the input is up-sampled to period Δ_1, then the resulting system can be described, without loss of generality, in innovations form (Anderson & Moore, 1979; Goodwin & Sin, 1984) as follows:

$$x_{k+1} = Ax_k + B\bar{u}_k + K\varepsilon_k \tag{1}$$
$$y_k = Cx_k + \varepsilon_k \tag{2}$$

where $x_k \in \mathbb{R}^n$, $\bar{u}_k \in \mathbb{R}^1$, $y_k \in \mathbb{R}^1$, $\varepsilon_k \in \mathbb{R}^1$ are the state, plant input, plant output and innovations sequence having variance σ_ε respectively. Furthermore, assume the transfer function $C(zI - A)^{-1}B$ to have relative degree $d + 1 < n$. Hence, for $d = 0$, $CB \neq 0$ and for $d \geq 1$,

$$CA^iB = 0 \quad \forall i = 0, 1, \ldots, d-1; \qquad CA^dB \neq 0. \tag{3}$$

Additional assumptions are introduced as follows:

A.2 The discrete time transfer function from $\bar{u}$ to y is stable and minimum phase.

A.3 A uniform-interval-nearest-neighbour quantizer with 2^p levels is deployed.

A.4 All bits used in the quantizer are communicated between controller and plant over a serial link supporting b_r bits/s.

A.5 The communication channel is error free.

Note that, a quantizer which allocates p bits/sample introduces a transmission delay of period $\Delta_p = p\Delta_1$.

3. Feedback architecture and quantizer

The proposed architecture for the feedback system is shown in Fig. 1. In this figure, a superscript p denotes either a downsampled signal with period $p\Delta_1$ or a system that operates at period $p\Delta_1$. The architecture shown in Fig. 1 has the following degrees of freedom: C^{p1} (a controller which is driven by a signal with sample period Δ_1, which outputs a control every pth sample), $(1+L_p)$ and $(1+L_p)^{-1}$ (the channel coder and decoder), $Q^p(\cdot)$ a 2^p level quantizer having step size λ^p and H^p (providing feedback around the quantizer). For realizability L^p and H^p are constrained to be strictly proper. We define $s^p = \bar{v}^p + q^p$ where q^p denotes the quantization error sequence. At sample time $k = \ell p$, $\ell \in \mathbb{Z}^+$, the controller has knowledge of all past outputs (sampled at period Δ_1), that is $y_{\ell p}$, $y_{\ell p-1}$, $y_{\ell p-2} \ldots$. The controller then generates an input signal u_ℓ^p. This input signal is held for p samples. The up-sampled input signal is denoted as u_k. Note that $u_{\ell p+i} = u_\ell^p$, $i = 0, 1, \ldots, p-1$. After filtering by $(1+L^p)$ the input signal is quantized to 2^p levels which leads to a p bit representation. It takes $p\Delta_1$ s to transmit these p bits over the communication channel to the plant input thus satisfying the bit rate constraint. The signal is passed through $(1+L^p)^{-1}$, then a series to parallel conversion is applied followed by D/A conversion. This process produces a piecewise constant control signal constrained to the same 2^p levels. This signal is then passed through a p sample hold so that the plant input, $\bar{u}_k$, is constant for p successive samples. During this period, the next p bits are received, allowing the next plant input to be reconstructed, and so on. The total delay between sample time, $k = \ell p$, (the time that a sample of the output is taken) and the first time that the resultant control, $u_{\ell p}^p$, effects the output of the plant is $(d + p + 1)$ samples. Note that, due to the p sample hold nature of the input, the output at sample period Δ_1 will be cyclostationary with period p.

We assume a uniform quantizer, which is characterized by the step size between quantization levels. $Q^p[\cdot]$ denotes the quantization operation. The quantization error is defined as

$$q^p = \bar{v}^p - Q[\bar{v}^p] \tag{4}$$
$$= F_\lambda^p[\bar{v}^p] \tag{5}$$