Control Engineering Practice 55 (2016) 149–161

Contents lists available at ScienceDirect

Control Engineering Practice

journal homepage: www.elsevier.com/locate/conengprac

FPGA-based optimal robust minimal-order controller structure of a DC–DC converter with Pareto front solution

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ARTICLE INFO

Article history:
Received 29 January 2016
Received in revised form
21 June 2016
Accepted 23 June 2016
Available online 25 July 2016

Keywords:
FPGA
DC–DC converter
multi-objective optimization
$\mathfrak{H}_\infty$ robust control

ABSTRACT

This paper presents multi-objective optimization-based robust controller design of a DC–DC boost converter, controlled with FPGA (Field Programmable Gate Array). The main aim of the proposed design technique is to obtain a fixed and low-order robust controller which is reliable and easy to implement on a low-cost real-time digital system. The improved proposed control design method with direct closed-loop pole position assessment using metric L_2, is based on robust optimal regional closed-loop pole assignment technique. The optimal solution has been obtained using multi-objective Pareto front search genetic algorithm. This paper also presents simulated and practical experimental results with implemented optimized robust controller on FPGA, controlling the DC–DC boost converter. For the sake of comparison with the proposed controller design method, an additional auto-tuned PID controller has been designed along with robust controllers based on mixed sensitivity loop-shaping method.

1. Introduction

DC–DC switching power converters are widely used in modern power conversion applications, such as: DC motor drives, power supply systems, uninterruptable power supplies, battery applications, telecommunications etc. Their widespread usage is due to high power conversion efficiency and a variety of possible applications (Ribes-Mallada, Leyva & Garcés, 2011; Yu, Qian & Lai, 2008; Kim, Kim, Min, Yoo & Kim, 2009; Sedaghati, Nahavandi, Badamchizadeh, Ghaemi & Fallah, 2012; Iqbal, Mekhilef, Soin & Omar, 2011). Nowadays, clean energy without pollution, such as photovoltaic (Wai, Wang & Lin, 2008), fuel cell (Wai & Duan, 2005), wind energy (Wai, Lin & Chang, 2007), etc., have become significant energy sources. Due to characteristics of clean energy sources, the generated power is affected by natural environment, while the output voltage is easily influenced by load variations. DC–DC switching converters also have other disadvantages such as: uncertainty of electronic elements, un-modeled dynamics, and continuous and discontinuous conduction mode, which altogether reflect the high nonlinearity of such converters. Un-modeled dynamics is also a consequence of averaging linearization methods (Calvente, Guinjoan, Martinez & Poveda, 1994; Wang, Li & Ma, 2014; Middlebrook & Ćuk, 1977).

Different linear control methods (Olm & Biel, 2010; Hsu & Lee, 2011; Cao, Ding, Wang & Chen, 2015; Ata & Coban, 2014; Chander, Agarwal & Gupta, 2010) have been applied to deal with disadvantages like un-modeled dynamics and uncertainty of elements, to reduce disturbance sensitivity of the output voltage, and to increase robustness and reliability of the converter (Khosroshahi, Abapour & Sabahi, 2015). Some improvements have been achieved with non-linear control methods, which have already been used for DC–DC converter applications in the last several years, such as control methods based on fuzzy systems (Lam, Lee, Leung & Tam, 2001; Saifia, Chadli, Labiod & Karimi, 2012), backstepping, and sliding mode techniques (Wai & Shih, 2011) combined with adaptive laws i.e. Oucheriah (2014). The latter technique mostly suffers from the chattering effect with varying parameters. Despite the fact that good results have been achieved, nonlinear design methodologies are still a challenging control design, due to much more rigorous and less general mathematical techniques for obtaining the desired dynamical behavior of a nonlinear system. *Model Predictive Control* (MPC) methodology, as a part of linear control theory, has also been applied several times to DC–DC converters and other similar applications (Spinu, Oliveri & Lazar, Storace; Yang, Li, Zhang & Xi, 2012; Wang & Boyd, 2010) implemented on FPGA. The main strength of the MPC methodology is on-line optimization of control cost function, which is optimized in every control-loop iteration (Wang & Boyd, 2010). At the same time, this is also a significant drawback due to high computational effort of on-line optimization. Sampling times of MPC controllers with on-line QP optimization, even on FPGAs, do not fall below the limit of 5 ms (Yang et al., 2012). Since MPC

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http://dx.doi.org/10.1016/j.conengprac.2016.06.016
0967-0661/

control is based on finite horizon cost function optimization, it also suffers from the stability issue of finite horizon (Chen, 2010).

High bandwidth of a DC–DC converter is of great interest, because of fast dynamical disturbances that can occur at output and input voltage, since a converter with a fast dynamic has lower reaction time to disturbances. When dealing with high dynamical behavior of a DC–DC converter, conventional microprocessors are not fast enough to evaluate control algorithms in real-time. Real-time evaluation of the control loop is the main prerequisite of stable digital control. FPGAs (Field Programmable Gate Arrays) have been used for quite a while now for guaranteeing real-time control evaluation in different control applications, including applications of DC–DC converters (Hsu & Lee, 2011; Chander et al., 2010; Monmasson & Cirstea, 2007; Ramadan, El-bardini & Fkirin, 2014; Soares dos Santos & Ferreira, 2014; Milanovič, Truntic & Slibar., 2005; João, de Carvalho, Andrés, Valentin & de Oliveira, 2013). The main advantage of FPGA against ASIC CPUs is parallel data processing, which can greatly decrease control loop evaluation time, as already presented in previous work (Sadek, Sarjaš, Svečko & Chowdhury, 2015). Thus, the main focus of this paper is the design of a fixed structure low-order robust controller, which is reliable and easy to implement on the lowest-cost FPGA device with very limited resources.

Linear optimal robust low-order controller design approach has been researched, due to design constraints of different non-linear control methods and constraint of significant computational cost. The possibilities of increasing robustness and performance in linear control theory have been fairly well explored to date. The most well-known metrics used in robust control theory H_∞, H_2 and μ synthesis have been introduced by several authors such as (Doyle, Francis & Tannenbaum, 1990; Doyle, Glover, Khargonekar & Francis, 1989; Kwakernaak, 1991; McFarlane & Glover, 1990; Zhou, Doyle & Glover, 1997). Because of certain significant disadvantages of the abovementioned robust control theory metrics, new improvements have been achieved with further research by (Chowdhury, Sarjas & Svecko, 2011; Gahinet & Apkarian, 2007; Henrion, Šebek & Kučera, 2003; Yang, Gani & Henrion, 2007). These improvements require complex mathematical formulations which in some cases fail to provide unique solutions. These drawbacks among others have led to research of bio-inspired computing and optimization-based control design techniques, known as *Heuristic* methods. *Heuristic* approaches seem to be superior in solving complex optimization problems (see (Soltanpour & Khooban, 2013; Mahale & Chavan, 2012; Binitha & Sathya, 2015)) to obtain optimal controllers of different structure especially when traditional *exact* method fail to provide unique solution. Some improvements in optimization-based robust controller design, based on robust polynomial synthesis has already been presented by (Sarjaš, Svecko & Chowdhury, 2011; Sarjaš, Svecko & Chowdhury, 2012). Optimal robust polynomial synthesis of fixed low-order controller, considering desired dynamical behavior and robustness cost function, has been originally researched by (Sarjaš, Chowdhury & Svecko, 2015). The main idea of the original work is to optimize matching cost function of the closed loop characteristic polynomial against reference characteristic polynomial as well to guarantee robustness, using multi-objective evolutionary optimization technique. A big advantage of such design method over standard robust controller design methods i.e. H_∞, H_2 and μ synthesis is independence of a controller structure and order. Standard robust controller design techniques reflect by high order controller, which is highly dependent of a system and its uncertainty.

The main contribution of this paper is a fixed and low-order controller structure design technique for robust controller design, which is suitable for implementation on the lowest-cost FPGA running at a very high sample rate. Such design technique is also applicable with various controller and plant structures. The proposed design technique originates from robust pole placement synthesis (Sarjaš et al., 2015) with difference of direct pole position assessment. The benefit of the proposed principle over the principle in the original work is the additional knowledge of closed-loop stability based on pole position. Multi-objective optimization approach is required to find Pareto optimal solutions of a fixed low-order robust controller, due to two limitations that prevents finding an *exact* solution of a robust controller. The first limitation is based on non-existence of an *exact* Diophantine equation solution. The second limitation is based on L_∞ metric, which considers both poles and zeros for assessing robustness of a closed-loop system. Therefore, we can't guarantee robustness of the closed loop system by selecting reference closed-loop poles. By using multi-objective optimization technique, it is possible to find an optimal robust controller regardless of any limitation. Robustness optimization criteria have been derived from the standard H_∞ mixed sensitivity problem based on the uncertainty model of the DC-DC power converter. Essential for controller design is pole placement criteria based on the residual between direct closed-loop system pole positions and selected characteristic polynomial pole positions, weighted with the Euclidean distance metric L_2. Some other nonlinear constraints have also been considered throughout the optimization procedure in terms of closed-loop pole and optimization parameter restrictions. Such technique allows the design of a fairly simple and robust controller with fixed order, which can be arbitrary selected at the beginning of the design procedure. It allows for simple implementation and low computational effort of the controller on low-cost real-time digital systems.

This paper is organized as follows. The second section describes an uncertain model of a DC–DC boost converter, considering tolerances of electronic elements as well as large changes of load resistance to consider output disturbances. Section three summarizes robustness assessment of a mixed-sensitivity problem, presented as standard H_∞ problem for the uncertain model obtained in section two. Section four presents an optimal pole placement technique based on direct pole position assessment. Section five discusses the benefits of using a multi-objective optimization method where Pareto front solution is conducted. It also presents the objective functions and the design procedure used in the experimental section. Complete experimental results are presented in section six, using the proposed optimization-based robust controller design method. Experimental results include a simulation analysis of the obtained controller, as well as practical results obtained on a real-time system of the DC–DC boost converter and FPGA. Additional mixed-sensitivity loop-shaping based robust controllers and non-robust PID controller have been designed for comparison, and have been tested practically and by simulation. The numerical instability problem of a high-order robust transfer function implemented on a real-time system is also presented.

2. Uncertain system modeling

This paper is mostly focused on linear robust control of a DC–DC boost converter, based on a dynamical model of the converter depicted in Fig. 1. A general nonlinear time-variant model of a DC–DC boost converter, considering real capacitor and inductor, has been obtained directly in the state-space framework: