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# Optimal stabilization of constant power loads with input LC-filters

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ABSTRACT

This contribution examines fundamental performance limitations of active stabilization of constant power loads with input LC filters. In terms of the load input admittance, stabilization is posed as a linear $H_\infty$ optimization problem, where the influence of stabilization on power control performance is minimized while meeting stability and robustness constraints. It is shown that the bandwidth of power control is upper limited by the resonance frequency of the input filter and that additional feedforward controllers can be used to individually shape reference tracking and disturbance rejection. Optimal results are verified through simulations using two different stabilization schemes.



## 1. Introduction

As traditional hydraulic and pneumatic devices to an increasing extent are being replaced by electric motor drives, stability problems in connection with constant power loads (CPLs) fed through input LC filters are gaining interest in, for example, automotive, aerospace and marine applications (Emadi, Khaligh, Rivetta, &, Williamson, 2006; X.Y. Liu & Forsyth, 2008; Rivetta, Emadi, Williamson, Jayabalan, & Fahimi, 2004; Sudhoff, Glover, Lamm, Schmucker, & Delisle, 2000). With high bandwidth control of power electronic converters, the CPL keeps the power unaffected by dc-link voltage variations. The load therefore behaves like an incremental negative resistance, which may destabilize the poorly damped input filter. If the system cannot be stabilized passively, through modification of the physical input filter as described in Cespedes, Beechner, Xing, and Sun (2010) and Middlebrook (1976), active stabilization modifying the load power characteristics is required. Even though the state feed-forward stabilizing controller (SFSC) (Xinyun Liu & Forsyth, 2008) and the method in Lee and Sul (2009) include the inductor current, most proposed stabilization schemes modify the load power purely as functions of the dc-link voltage, which can be interpreted as simulating additional virtual resistance or capacitance of the load. Whereas methods like the Non-linear System Stabilizing Controller (NSSC) (Glover & Sudhoff, 1998; Jänecke, 1992; Sudhoff, Corzine, Glover, Hegner, & Robey, 1998) or the method proposed in Magne, Marx, Nahid-Mobarakeh, and Pierfederici (2012) implement the nonlinear control laws required for virtual component simulation, stabilization schemes usually apply approximate linear control laws. By this latter case, the controllers simply consist of a high-pass filter and a gain. For motor drives, such linear controllers have been proposed to affect the load power by modifying either the torque reference (Mosskull, Galic, & Wahlberg, 2007; Walczyna, Hasse, & Czarnecki, 1996), the current reference (Bae, Cho, & Sul, 2001; Liu, Forsyth, & Cross, 2007; Liu & Forsyth, 2005; Liu, Fournier, & Forsyth 2008; Mosskull, 2005a, 2005b; Pietiläinen, Harnefors, Petersson, & Nee, 2006) or directly the motor voltage reference (Delemontey, Jacquot, Iung, De Fornel, & Bavard, 1995; Hinkkanen, Harnefors, & Luomi, 2007; Mohamed, Radwan, & Lee, 2012). In Walczyna et al. (1996) and Mohamed et al. (2012), the stabilization controllers are actually based on the capacitor current instead of the dc-link voltage, but in the latter publication it is shown how to derive the capacitor current from the dc-link voltage in case the current is not available for measurement.

Although active stabilization does not require any hardware modification, it however introduces a disturbance to nominal power control. Stabilization therefore should be designed to reach required stability margins with minimal power modification. For proposed stabilization schemes, power control performance is usually only evaluated through visual inspection of a few simulations. To strengthen performance evaluation, this contribution derives explicit expressions for the power disturbance due to stabilization in terms of the external excitation signals supply voltage and power reference. These expressions are then used to examine the boundaries of achievable performance of active stabilization by posing stabilization as an optimization problem, where the power disturbance is explicitly minimized, subject to meeting requirements on stability margins. The optimization is done in terms of the load input admittance,

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which describes the effect of any stabilization scheme modifying the load power as a function of dc-link voltage. By also optimizing feedforward controllers from supply voltage and power reference, the derived results represent the optimum for any stabilization scheme using any combination of filter quantities for stabilization. Both power reference tracking and rejection of supply voltage disturbances are considered and minimization is done with respect to $H_\infty$ norms at various operating conditions. For reference tracking, also $H_2$ optimal stabilization is analytically derived.

In order to verify the results, the derived optimal stabilization is realized and simulated with an example induction motor drive using two different approaches, namely torque and voltage reference stabilization. Additional feed-forward control is also implemented and evaluated.

The paper is organized as follows: Section 2 presents the CPL stability problem and derives models to be used for stabilization analysis and design. In Section 3, stabilization is posed as an optimization problem, which is solved in Section 4. The obtained results are verified through simulations in Section 5 and the paper is finally summarized in Section 6.

## 2. Modeling

Fig. 1 shows a constant power load, exemplified by an induction motor drive, connected to a power supply via an input LC filter. In this section, a linear feedback model of this system is derived, to be used for analysis and stabilization design.

### 2.1. Constant power instability

The CPL in Fig. 1 will be represented by its consumed power $P$, which can be expressed in terms of the dc-link voltage $U_d$ and the dc-link current $i_d$ as

$$P(t) = U_d(t) i_d(t). \tag{1}$$

The load is connected to the (ideal) supply voltage $E$ via an input LC filter, which affects the dc-link voltage according to

$$U_d(t) = G_E(p)E(t) - Z_{DC}(p) i_d(t), \tag{2}$$

where the transfer functions $G_E$ and $Z_{DC}$ are given by

$$G_E(s) = \frac{1}{s^2LC + sRC + 1}, \quad Z_{DC}(s) = \frac{sL + R}{s^2LC + sRC + 1}. \tag{3}$$

The input filter is added to the CPL to suppress supply voltage harmonics, but also to reduce current harmonics generated by the load. From Eq. (2) it follows that the supply voltage $E$ affects the dc-link voltage $U_d$ via the filter $G_E$, which also is the transfer function from dc-link current $i_d(t)$ to inductor current $i(t)$. The bode plot of $G_E$ in Fig. 2 (blue curve) shows that the LC filter offers good suppression of high frequency harmonics (small filter gain). However, since the filter resistance $R$ is very small, to minimize copper losses, the LC-filter is poorly damped and has a significant

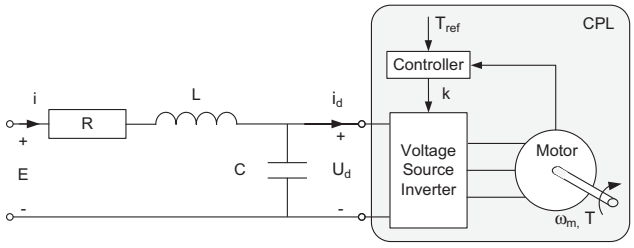


**Fig. 1.** A CPL, which in the figure is represented by a motor drive, connected to a power supply via an input LC input filter. The input filter is needed to suppress supply voltage ripple but also to suppress current harmonics generated by the load.

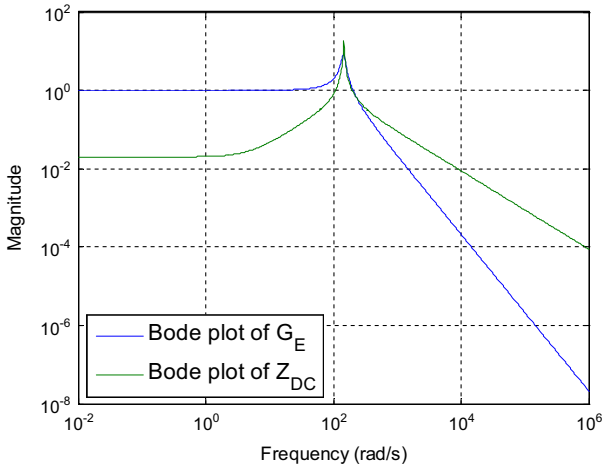


**Fig. 2.** Input filter transfer functions $G_E$ (blue) and $Z_{DC}$ (green). The filter offers good suppression at high frequencies but contains a significant resonance peak at the frequency $\omega_0 = 1/\sqrt{(LC)}$. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

resonance peak at the frequency $\omega_0 = 1/\sqrt{LC}$. The damping factor $\zeta$ of the filter can be calculated as $\zeta = R/2\sqrt{C/L}$.

Due to the power Eq. (1), the described system is non-linear. To be able to use design methods for linear systems, Eq. (1) is therefore linearized to give the following representation of the dc-link current, where $P_0$ and $U_{d0}$ are the operating point power and dc-link voltage:

$$i_d(t) = \frac{1}{U_{d0}} P(t) - \underbrace{\frac{P_0}{U_{d0}^2}}_{\triangleq Y_0} U_d(t). \tag{4}$$

In Eq. (4), the notation $Y_0$ was introduced for the input admittance (relation between dc-link current and voltage) of an ideal CPL, which follows since the power $P(t)$ of such a system is independent of the dc-link voltage. Consequently, the ideal CPL behaves like a resistance equal to $R_0 = 1/Y_0 = -U_{d0}^2/P_0$ at the LC filter output terminals. At positive power, the equivalent resistance $R_0$ is negative and therefore decreases damping of the system. This is evident from the following expression of the damping factor of the filter combined with the ideal CPL, where $\zeta$ is the damping factor of the filter (see e.g. Bae et al., 2001).

$$\zeta_{drive} = (1 + Y_0 R)^{-\frac{1}{2}} \left( \zeta + \frac{1}{2} Y_0 \sqrt{\frac{L}{C}} \right) \approx \zeta + \frac{1}{2} Y_0 \sqrt{\frac{L}{C}}. \tag{5}$$

With increasing power, the destabilizing effect of the CPL eventually causes instability of the interconnected system, i.e. with $\zeta_{drive} < 0$.

*Remark:* Note that the load admittance equals $Y_0$ in Eq. (4) as long as the load power is independent of the dc-link voltage. That is, the power does not necessarily have to be perfectly constant to cause instability. In this contribution, the term CPL will therefore be used for systems, where the power is independent of the dc-link voltage.

*Remark:* Note that the quantities in the linearized Eq. (4) represent deviations from an operating point (as opposed to Eq. (1)), although not explicitly indicated by the notation.

### 2.2. DC-link voltage feedback

In order to avoid the CPL instability, it is clear that the load input admittance must be modified (compared to $Y_0$). That is, the response in dc-link current to variations in dc-link voltage must be changed. The interface of the load to the filter is the consumed