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Plasma-activated direct bonding of diamond-on-insulator wafers to thermal oxide grown silicon wafers

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ABSTRACT

Diamond-on-insulator (DOI) wafers featuring ultrananocrystalline diamond are studied via atomic force microscopy, profilometer and wafer bow measurements. Plasma-activated direct bonding of DOI wafers to thermal oxide grown silicon wafers is investigated under vacuum. DOI wafer with chemical mechanical polishing (CMP) on the diamond surface makes a poor bonding to silicon wafers with thermal oxide. Our results show that plasma enhanced chemical vapor deposition of silicon dioxide on top of the DOI wafer, CMP of the oxide layer and annealing are essential to achieve very high quality direct bonding to thermal oxide grown on silicon wafers. Plasma activation results in the formation of high quality bonds without exceeding 550 °C in the direct wafer bonding process.

1. Introduction

Diamond is an attractive alternate membrane material to silicon for microelectromechanical systems (MEMS) applications because of its superior mechanical, electrical and thermal properties [1]. High Young's modulus, low dielectric constant, very large thermal conductivity and high dielectric strength of diamond (see Table 1) are all in favor of diamond as a strong candidate to be used for electromechanical transducers. Because of its high radiation resistance, chemical inertness and extreme hardness, diamond is best suited for high temperature, high power and radiation-hard devices [1]. Therefore, diamond is a promising membrane material for improving performance and reliability of capacitive micromachined ultrasonic transducers (CMUTs) [2].

The CMUT cavity is formed with the patterned etch of the thermally grown SiO_2 insulation layer on the silicon wafer. The top surface of this patterned wafer is directly bonded to commercially available silicon-on-insulator (SOI) wafer under vacuum and single crystal silicon device layer of the SOI wafer becomes the membrane sealing the cavities following the removal of the bulk silicon and buried oxide [3]. Using diamond-on-insulator (DOI) wafer instead of SOI wafer can form diamond membranes with a similar process flow if the direct bonding of diamond and patterned silicon dioxide surfaces is successfully achieved. In this respect, the direct bonding potential between diamond and silicon dioxide surfaces should be explored for full wafer to wafer contact.

Although direct bonding of silicon and silicon dioxide surfaces is accomplished and readily employed in the production of silicon membranes [3], the bonding of diamond and silicon dioxide surfaces has not been explored yet. This is due to (1) lack of high quality diamond films with small grains and smooth surfaces, (2) extreme hardness of diamond surface reducing the smoothing performance of chemical mechanical polishing (CMP), and (3) plasma activation becoming less effective due to high chemical stability of carbon bonds in diamond. These facts make the direct wafer bonding of diamond to SiO_2 very challenging. The deposition of a SiO_2 interlayer is widely used to achieve the bonding of dissimilar materials or materials with surface irregularities such as roughness [4]. The wafer bonding of diamond and silicon surfaces is achieved with a high temperature oxide (HTO) deposited as an additional layer on diamond [5]. Complete direct bonding of diamond to silicon was achieved under a uniaxial mechanical stress of 32 MPa in a dedicated ultrahigh vacuum chamber at annealing temperatures above 1150 °C with some cracks on the diamond film [6]. Plasma-activated direct bonding of silicon and diamond-like-carbon (DLC) with an annealing temperature of 450 °C was used to fabricate silicon-on-diamond structure with hydrogen-induced layer transfer method [7].

Recently, ultrananocrystalline diamond (UNCD) has become commercially available on Si wafers, featuring smaller grain size and surface roughness (3–4 nm) than conventional diamonds (Advanced Diamond Technologies (ADT), IL, US). The surface roughness of UNCD is further reduced below 1 nm by CMP. In this work, we investigate the 4-in UNCD DOI wafers via atomic force microscopy, profilometer and wafer-bow measurements. We study the direct bonding of UNCD DOI wafers onto SiO_2 grown Si wafers which is a critical step to have diamond membranes over vacuum sealed cavities.

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Table 1
Material properties of Si, SiO_2, UNCD, and diamond at room temperature [1]: Young's modulus (E), density (ρ), Poisson's ratio (v), thermal conductivity (k), hardness (h), thermal expansion coefficient (α), dielectric constant (ϵ), and dielectric strength (E_{ds}) are shown for comparison.

	Si	SiO_2	UNCD	Diamond
E (GPa)	160	73	850	1050
ρ (kg/m^3)	2332	2200	3300	3520
v	0.29	0.17	0.1	0.2
h (kg/mm^2)	1000	1000	10000	10000
k ($W/m-K$)	151	1.4	1200	2000
α ($10^{-6}/K$)	2.5	0.5	0.8	0.8
ϵ	11.7	3.8	5.7	5.7
E_{ds} (10^5V/m)	3.7	100	100	100

2. Experiment

Silicon wafers with SiO_2 are realized via thermally oxidizing base prime <100> silicon wafers (4-in, 5–10 Ω cm, 525 ± 25 μm) at 1000 °C. The oxide thickness of 1.5 μm is achieved using a combination of wet and dry oxidation. Initial and final stages of the oxidation are performed with dry oxidation whereas in-between wet oxidation is employed. Oxidation temperature of 1000 °C is used to have good control over the thickness and uniformity of the oxide over the wafer. The average oxide thickness of 9-point measurements across the wafer using spectroscopic reflectometer (NanoSpec, Nanometrics, CA, US) is within %1 of the target thickness of 1.5 μm and the standard deviation of oxide thickness is less than 4 nm across the wafer. The wafers S_{1-4} and A_1 have these thermal oxide layers (see Table 2).

Commercially available DOI wafers feature UNCD layer with 300–350 MPa compressive stress and thickness variation of %20 over the whole wafer. A compressive stress in the membrane material will cause buckling of the membrane and will degrade device performance. Thickness variation will cause frequency shift from the intended frequency range of operation. Therefore, DOI wafers with custom deposited UNCD layer are used instead of the regular DOI wafers. Diamond-on-insulator wafers that are custom prepared by ADT feature 0.5 μm UNCD layer with minimum residual stress (−50 MPa<S<50 MPa), smallest grain size and surface roughness (R_a) below 1 nm over 1 μm thermal oxide grown <100> base silicon. The low surface roughness is achieved with the chemical mechanical polishing of the UNCD surface by ADT. The DOI wafer labeled B_1 is formed aforementioned.

The DOI wafers without the final CMP step are used to study the effect of deposited SiO_2 as an intermediate layer on direct bonding. In this respect, DOI wafers, C_1 and D_1, have additional SiO_2 deposited via plasma enhanced chemical vapor deposition (PECVD) at 300 °C (STS PECVD, Surface Technology Systems, Newport, UK). The initial deposited oxide thickness of 0.5 μm is reduced down to 0.1 μm, by properly adjusting the CMP duration based on the initial processing of the test wafers (<100> base silicon wafer with 0.5 μm PECVD oxide). Because of the multi-layer nature of the DOI wafers, the spectroscopic reflectometer measurements of the remaining oxide thickness are performed on the test wafers. The CMP is performed by Axus Technology (Chandler, AZ, US) using Semi-Sperse 25-E slurry (Cabot Microelectronics, IL, US) diluted with water (slurry:water) (1:1) on Westech Model 472 CMP System (Speedfam-IPEC, Japan). Wafer cleaning of the slurry remaining after the CMP is performed on OnTrack DSS-200 Post CMP Cleaner (OnTrack, CA, US). The wafer C_1 was kept as is whereas the wafer D_1 has been annealed at 400 °C under N_2 flow in Thermco furnace (Thermco Systems, West Sussex, UK) for 19 hours to densify the wafer (see Table 2). This annealing temperature higher than the oxide deposition temperature of 300 °C and longer duration of annealing are employed to ensure the extraction of trapped H_2 gas in the PECVD oxide layer [8]. The annealing is performed after the CMP in order to (1) facilitate the diffusion of the trapped gas through a thinner oxide layer, and (2) enhance the surface cleanliness with the better removal of small size slurry particles on the unannealed PECVD oxide surface rather than annealed oxide surface. Higher annealing temperatures are avoided to protect the diamond layer from reacting with present O_2 molecules in the open-ended atmospheric furnace and to release the trapped H_2 gas in the oxide layer in a slow, controlled process [8].

Table 2 summarizes all the wafers reported in this study and lists their constituent layers. The surface roughness and the wafer bow are measured for each wafer, and given in Tables 3 and 4, respectively. The wafer pairs of (S_1 and A_1), (S_2 and B_1), (S_3 and C_1), and (S_4 and D_1) are direct bonded to form A_1^1, B_1^2, C_1^3, and D_1^4, respectively. The quality and stability of these direct-bonded pairs are analyzed by scanning acoustic microscopy (SAM).

Table 2
Description of wafer pairs: IDs, bonded wafers, wafer constituents and processing steps.

ID	Bonded wafers	Wafer constituents on top of silicon wafer	Processing steps
A_1^1	S_1	1.5-μm thermal SiO_2	$Cleaning_1$
	A_1	1.5-μm thermal SiO_2	$Cleaning_1$
B_1^2	S_2	1.5-μm thermal SiO_2	$Cleaning^1$
	B_1	1-μm thermal SiO_2	CMP
		0.5-μm UNCD	and $cleaning_2$
C_1^3	S_3	1.5-μm thermal SiO_2	$Cleaning_1$
	C_1	1.-μm thermal SiO_2	CMP
		0.5-μm UNCD	and $cleaning_3$
		0.1-μm PECVD-SiO_2	
D_1^4	S_4	1.5-μm thermal SiO_2	$Cleaning_1$
	D_1	1-μm thermal SiO_2	CMP,
		0.5-μm UNCD	densification,
		0.1-μm PECVD-SiO_2	and $cleaning_3$

3. Results and discussion

3.1. Characterization

The atomic force microscopy (AFM) (5500 LS, Agilent Technologies, Santa Clara, CA, US) measurement of a 10×10 μm^2 thermal oxide surface gives a root-mean-square (RMS) roughness (R_q) of 1.5 Å and a roughness average (R_a) of 1.2 Å whereas that of PECVD SiO_2 surface after CMP gives R_q and R_a of 4.5 Å and 2.9 Å , respectively. PECVD SiO_2 was smoothened by CMP; however, the polished oxide was still rougher than the thermal grown SiO_2. AFM image of UNCD surface after CMP is given in Fig. 1, and surface roughness values for R_q and R_a are 16.5 Å and 10.7 Å, respectively. Surface roughness of DOI wafers (B_1, C_1, and D_1) is further studied across the 4-in wafers using Dektak 8 profilometer (Veeco, Plainview, NY, US) with 0.2 μm stylus attached.

Table 3
Surface roughness measurements of UNCD wafers: B_1, C_1, and D_1. R_q is the RMS roughness and R_a is the roughness average, given in the brackets. All units are in Angstrom (Å).

Wafer ID	B_1	C_1	D_1
Position (cm, cm)	$R_q(R_a)$ Å(Å)	$R_q(R_a)$ Å(Å)	$R_q(R_a)$ Å(Å)
A(0,0)	11.0(8.5)	9.8(7.9)	9.8(8.0)
B(−1,1)	13.2(10.2)	10.4(8.1)	13.4(11.0)
C(−2,2)	12.6(10.0)	8.5(10.7)	8.8(7.0)
D(−3,3)	12.7(10.1)	8.7(7.0)	10.3(8.3)
E(1,−1)	15.0(11.9)	10.0(8.0)	8.6(6.7)
F(2,−2)	16.0(13.1)	12.3(9.8)	10.6(8.5)
G(3,−3)	13.9(11.0)	9.6(7.6)	8.7(7.1)
K(0,−1)	16.3(12.6)	9.4(7.4)	15.1(12.4)
J(0,−2)	15.7(12.5)	9.0(7.2)	8.2(6.5)
I(0,−3)	13.2(10.4)	8.9(7.2)	8.6(6.8)
H(0,−4)	15.7(12.3)	12.2(9.8)	11.3(9.0)