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Improved electrical properties of SiC wafer with defects covered by free standing graphene

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ABSTRACT

As a single crystal SiC is grown, defects and dislocations occur due to many reasons. In particular, defects such as micropipes and micropores that are generated during the growth of single crystal SiC ingot have irregular locations and sizes. These defects continue to exist after the manufacturing process and undermine the properties of single crystal SiC wafer. Moreover, they lower the electrical properties of the wafers and can even cause detrimental damages after being applied in devices.

We combined single crystal SiC wafer and graphene with a floating method in order to use graphene as a bridge to connect the SiC bonding that is broken due to defects such as micropipes and micropores in single crystal SiC wafer. In this process, we characterized the layers of graphene needed, ranging from monolayer to multilayer, to cover micropipes and micropores of various sizes. As a result of measuring the thermoelectrical conductivity of single crystal SiC wafer combined with monolayer graphene up to temperatures of 400 °C, we observed electrical conductivity that was two or three orders higher than that of the SiC wafer alone. In addition, the connection between the SiC and the graphene was stable.

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1. Introduction

As silicon carbide (SiC) has better electrical and thermal properties including band gap energy, breakdown field and thermal conductivity than Si as well as outstanding chemical stability, much research is underway to use it in the field of semiconductor for high temperature and high power environment [1–3]. The SiC used in this field is a single crystal 4H SiC of α phase having hexagonal structure, and there are two methods of growing single crystal SiC including vapor phase growth process and liquid phase growth process. Among the methods, physical vapor transport (PVT), one of the vapor phase growth processes, is most frequently used. Because it is superior in fabricating a large-diameter wafer and has the advantage of a high growth rate. During the growth of single crystal SiC by the PVT method, micropipe and micropore defects and screw and edge dislocations occur due to the status of seed surface, stress by the growth temperature gradient and impurities of the source, SiC powder [4–7]. In particular, the micropipe is a unique defect in the growing of single crystal SiC that continuously occurs until the growth of the SiC ingot is finished. These micropipe and micropore not only reduce the yield rate of single crystal SiC, but also lower its electrical and thermal properties, thereby posing an obstacle in the manufacturing of high power devices. Much research has been carried out in the past decades to diminish such defects, but a clear solution has yet to be developed.

Defects are problematic as they lower the properties of single crystal SiC. To think reversely, if the properties of single crystal SiC remain the same even if defects are existent, it is possible to be applied to devices. Based on this, we studied how to improve the properties of single crystal SiC wafer with defects. By combining single crystal SiC with graphene, we devised a method to supplement the defects.

Based on the research result of C. Berger and W. A. de Heer et al. who studied on the interaction between graphene and SiC substrate by growing epitaxial graphene on Si face of two polar faces (0001) and C face of $(000\bar{1})$ [8,9], it was proposed that graphene can create a strong covalent C–C or Si–C bond with the C or the Si terminal atom on the surface of SiC, which has carbon atoms arranged in a two-dimensional hexagonal lattice. In addition, graphene was thought to be able to create a strong bond that is structurally and mechanically stable as the Young's modulus reaches 0.5 TPa. Furthermore, due to graphene's highly desirable electrical properties including high electron velocity, high electric conductivity, and a low electronic scattering rate [10,11], we thought that it could contribute to improving the electrical properties of SiC by addressing the latter's issues with low electron mobility. We also believed that the size of high power and high temperature devices using single crystal SiC wafers could be reduced due to the high thermal conductivity of graphene. SiC wafers manufactured from the same single crystal SiC ingot can have different sizes and defect distributions depending on their location in the ingot. To effectively supplement the defects, we used a floating method to combine graphene in the desired locations. In addition, we combined different layers of graphene and confirmed the optimal number of layers for supplementing various

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defect sizes. We also measured the thermoelectrical conductivity of single crystal SiC combined with graphene to study the electrical behaviors and the effect of graphene on single crystal SiC wafer.

2. Experimental details

The single crystal SiC was grown by the PVT method under an Ar atmosphere at a growth temperature of 2300 °C. The grown SiC crystals were sliced approximately perpendicular to the growth direction into (0001) wafers. Graphene was grown on copper (Cu) substrate by chemical vapor deposition (CVD) using methane gas. As-grown graphene was separated from the Cu substrate by the dissolving of Cu etchant ($FeCl_3$ liquid). After dissolution, the graphene floating on top of the solution was transferred onto the SiC wafer. The SiC surface and graphene were more stably combined after the remaining liquid was evaporated through a baking process. To confirm the growth of graphene and the number of its layers, a Raman spectrometer (Jobin-Yvon, LabRam HR) with an excitation laser wavelength of 514.5 nm (Ar laser) was used at room temperature. Field emission scanning electron microscopy (FESEM, JEOL, JSM-7001F) was used to confirm the graphene covering according to the defect sizes of the single crystal SiC wafers. We used a thermoelectrical property measuring system (Ozawa science, RZ-2001) with a DC 4 point probe to measure the bonding stability and electrical conductivity according to the temperature increases on the SiC substrate combined with graphene and the SiC substrate without graphene.

3. Results and discussion

Fig. 1 is a schematic diagram of how to use graphene to cover the defects of SiC wafer. As seen in the figure, the size and location of the defects on the SiC wafer are irregular, and the electrical properties are lowered in the parts where SiC bonding is broken with micropipe defects penetrating through the wafer. To supplement these defects, we covered the micropipes or micropores on the wafer surface with graphene to bridge the broken SiC bonding. As graphene and the single crystal SiC wafer are combined using a floating method, the graphene does not get inside of the defect, but exists as freestanding graphene. We varied the number of graphene layers from a monolayer to multilayers and combined them with defects with sizes ranging from tens of μm to hundreds of μm in order to confirm the thickness of graphene that can sustain different defect sizes.

Fig. 2(a) shows the result of Raman spectroscopy used to analyze the formation and bonding of graphene after it was used to cover defects on the single crystal SiC wafer. Raman spectroscopy is frequently used because it can effectively characterize graphene according to the location and intensity of the Raman spectra peak. The Raman spectra of graphene consist of a 1350 cm^{-1}(D peak) occurring near the first-order zone boundary phonons, a 1580 cm^{-1}(G peak) by the sp2 phonon vibration and a 2670 cm^{-1}(2D peak) caused by the double resonance process of the phonon in the electronic band structure. Defects or impurities in graphene can be confirmed through the D peak. In particular, the formation of graphene and the number of its layers can be indicated by the 2D peak's position, shape, and width [12,13]. Our sample of graphene on the SiC wafer did not show a D-band, and the G-peak appeared near 1580 cm^{-1}. From this, we confirmed that our sample consisted of monolayer graphene without any defects. As the ratio of I_{2D}/I_G was approximately three, the grain size of the graphene was thought to be multi-μm. Other peaks that did not correspond to graphene also occurred in the analysis of the SiC wafer, appearing in the positions of 1514, 1615, and 1714 cm^{-1} [14,15]. The reason why SiC peaks were also observed in the Raman spectra of free-standing

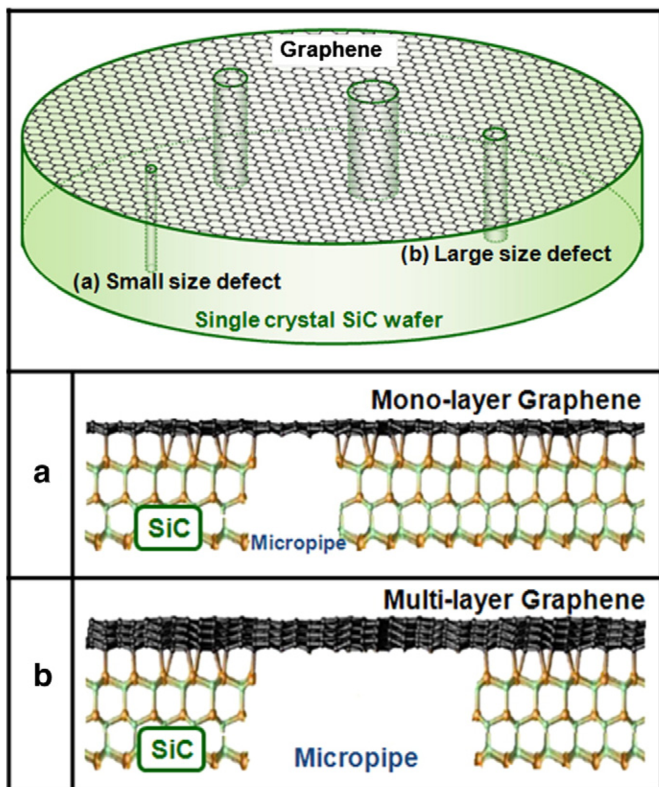

Fig. 1. Schematic diagram of different sizes of defects covered with graphene on a single crystal SiC wafer. (a) the number of graphene layer to cover small size micropipe and the form of graphene sustaining as a bridge (b) the number of graphene layers needed to bridge large sized micropipes.

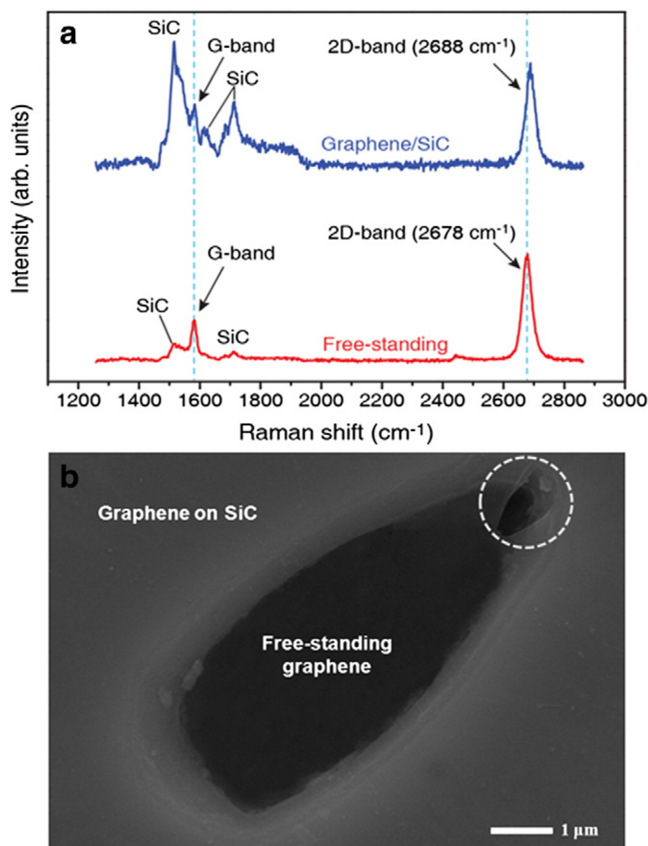

Fig. 2. (a) Comparison of Raman spectra between monolayer graphene that is free standing on the defect and monolayer graphene that is combined with single crystal SiC wafer. (b) SEM image of 10 μm sized defects on a single crystal SiC wafer covered with monolayer graphene.

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