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Plasma-activated direct bonding of patterned silicon-on-insulator wafers to diamond-coated wafers under vacuum

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ABSTRACT

Direct wafer bonding requires the surfaces to have low surface roughness ($R_a < 0.5$ nm) as well as to be free of any particles or contaminants. Meeting these requirements for wafers patterned with lithography and dry etching presents a serious problem in terms of removal of photoresist residue and etch-related particles, which would require expensive additional equipment to be removed. In this study, we propose the use of chemical mechanical polishing (CMP) to be performed after all lithography and dry etch process steps involving several masks are completed. To reduce the adverse effect of any remaining slurry that might reside in the etched structures, we also propose to reduce the maximum annealing temperature from 550 °C down to 300 °C. The effect of lower annealing temperature on bonding is compensated using a sequential plasma activation with 60 s of O_2 followed by 90 s of N_2 on contacting surfaces made of silicon dioxide to achieve successful wafer bonding. Initial plasma activation with O_2 additionally serves as a final cleaning step whereas the following activation with N_2 for an extended duration is to fully activate the surface for direct bonding. This proposed technique can motivate the use of direct wafer bonding for microfabrication of advanced MEMS devices.

1. Introduction

Direct wafer bonding has been a versatile tool due to the achievement of high bonding strength between the contacting surfaces, which is appealing for the microfabrication of MEMS devices for diverse applications [1–3]. Bonding of most processed wafers requires a low temperature bonding [1]. With the advent of plasma activation, direct wafer bonding can achieve almost the bulk strength in bonding silicon–silicon surfaces at low temperature [1]. Plasma activation is a powerful technique for hydrophilic wafer bonding [4]. Having silicon dioxide as one of the mating surfaces increases the effectiveness of plasma activation. However, having thick silicon dioxide on both surfaces reduces the maximum bond strength due to longer diffusion length for water between the contacting surfaces to reach the silicon [1]. The plasma increases the kinetics of water removal from the bonded interface due to plasma-induced porous oxide layer [1].

Grown diamond films present significantly high surface roughness for direct wafer bonding. Based on a smoothing process involving deposition, planarization and etching (DPE) steps, the surface roughness can be reduced down to 1.5 nm [5]. Recently, diamond surface roughness as low as 1.7 nm is achieved via CMP using silica-based slurry [6]. However, the surface roughness is still too large for direct wafer bonding [7]. Direct wafer bonding also requires chemical affinity of the bonding surfaces in addition to surface flatness and cleanliness [7]. Thanks to the plasma activation resulting in high bonding strengths for surfaces having silicon dioxide, bonding of dissimilar materials such as diamond and silicon dioxide can be achieved by using silicon dioxide as an interlayer [7]. In our earlier work, diamond has been used as a membrane material for the microfabrication of vacuum-sealed cavities with such an interlayer [8]. Recently, these cavities are employed in capacitive micromachined ultrasonic transducers (CMUTs) featuring diamond membranes [3,9]. However, meeting the criteria for the applicability of direct wafer bonding as a microfabrication technique becomes overwhelmingly difficult as the complexity of pre-processing of these wafers such as lithography and dry etching increases. In this study, we explore the use of plasma activated direct bonding of patterned silicon-on-insulator (SOI) wafers to diamond-coated wafers under vacuum. Influence of chemical mechanical polishing on patterned SOI wafers and bonding conditions such as high piston force and sequential plasma treatment for a longer duration is explored to achieve a successful direct wafer bonding.

2. Experiment

Silicon wafer (4-in, <100>, As-doped, <0.005 Ω cm, 525 ± 25 μm) having a thermal oxide thickness of 1 μm and SOI wafers (4-in, <100>, Si base: As-doped, <0.005 Ω cm, 475 ± 10 μm, buried oxide layer: 1 μm, Si device layer: As-doped, <0.005 Ω cm, 20 ± 0.5 μm) having a thermal oxide thickness of 1 μm are directly purchased from a wafer supplier (Silicon Quest International, CA, US). The description of the wafers used in this study is given in Table 1. The top oxide layer of

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Table 1
Description of wafer pairs.

ID	Bonded wafers	Layers	Preparation	Bonding conditions
A_1^1	S_1	SiO_2 (0.85 μm)	CMP	30 s N_2 plasma,
	A_1	UNCD (1 μm)	CMP	10 kN force,
		SiO_2 (0.55 μm)		550 C for 1 h
B_1^2	S_2	SiO_2 (1 μm)	CMP	30 s N_2 plasma,
		Si (20 μm)	Lithography	10 kN force,
		SiO_2 (0.85 μm)		550 C for 1 h
	B_1	NCD (1 μm)	CMP	
		SiO_2 (0.55 μm)		
C_1^3	S_3	SiO_2 (1 μm)	Lithography	30 s N_2 plasma,
		Si (20 μm)	CMP	10 kN force,
		SiO_2 (0.85 μm)		550 C for 1 h
	C_1	NCD^B (3.5 μm)	CMP	
		SiO_2 (0.55 μm)		
D_1^4	S_4	SiO_2 (1 μm)	CMP	60 s O_2 plasma,
		Si (20 μm)	Lithography	90 s N_2 plasma,
		SiO_2 (0.85 μm)		20 kN force,
	D_1	UNCD (1 μm)	CMP	300 C for 1 h
		SiO_2 (0.55 μm)		
E_1^5	S_5	SiO_2 (1 μm)	Lithography	60 s O_2 plasma,
		Si (20 μm)	CMP	90 s N_2 plasma,
		SiO_2 (0.85 μm)		20 kN force,
	E_1	MCD^B (0.7 μm)	CMP	300 C for 1 h
		SiO_2 (0.55 μm)		

the silicon wafer (S_1) is subject to chemical mechanical polishing (CMP) to reduce the surface roughness. SOI wafers (S_2 and S_4) are subject to CMP first followed by lithography and reactive ion etching (RIE) processes, whereas the other SOI wafers (S_3 and S_5) are patterned first followed by CMP. Based on the measured oxide etch rate of 300 nm/min with a ceria-based slurry (Cabot Microelectronics, IL, US), CMP is performed for 30 s reducing the initial oxide thickness of 1 μm down to approximately 0.85 μm for the silicon (S_1) and SOI wafers (S_2–S_5).

Silicon wafers (4-in, <100>) coated with different diamond types are used in this study. These diamond types are undoped ultrananocrystalline diamond (UNCD), undoped nanocrystalline diamond (NCD), boron-doped nanocrystalline diamond (NCD^B), and boron-doped microcrystalline diamond (MCD^B) (see Table 1). Other than UNCD-coated wafers supplied by ADT (Advanced Diamond Technologies, IL, US), all others are supplied by sp3 (sp3 Diamond Technologies, CA, US). All diamond-coatings are provided with minimum residual stress (-100 MPa < S < 100 MPa) due to the requirements of our potential device [9]. These diamond-coated wafers have SiO_2 deposited via plasma enhanced chemical vapor deposition (PECVD) method at 300 °C (PlasmaLab System 100, Oxford Instruments, UK). The initial deposited oxide thickness of 1 μm is reduced down to 0.55 μm by CMP for 90 s. These wafers are used in the bonding experiments (see Table 1).

Process steps used in the experiments are presented in Fig. 1. An SOI wafer with thermal oxide on top (Fig. 1(a)) is patterned with MASK1 to form the cavities using RIE of SiO_2 (Fig. 1(b)). Because of the hydrophilic nature of the oxide surface, dehydration of the wafer on a hotplate is performed. Additionally, the wafer is coated with hexamethyldisilazane (HMDS) to promote resist adhesion. To limit the adverse interaction of HMDS and the photoresist, separate spin coaters are used. The photoresist (AZ4533, Clariant Corp., US) is coated for a thickness of 3.3 μm (4000 rpm, 1000 rpm/s, 50 s). High acceleration rate is required to achieve the desired photoresist profile. A prebake is performed on a hotplate (100 °C, 200 s). Using MASK1, the photoresist is exposed at a constant dose of 45 mJ under vacuum contact using a mask aligner (EVG620, EVGroup, Austria), and then is developed using a developer (AZ400K, Clariant Corp., US) for 100 s. The oxide layer is completely removed inside the cavity with RIE (STS RIE, Surface Technology Systems, Newport, UK). The photoresist is removed using O_2 plasma and piranha cleaning (4:1 mixture of H_2SO_4:H_2O_2, 130 °C for 15 min). The cross-section of a SOI wafer processed as described is depicted in Fig. 1(b). Using MASK2 to separate the cavities, RIE etch of SiO_2 followed by deep reactive ion etching (DRIE) of Si device layer is performed (Fig. 1(c)). A photoresist thickness of 3.3 μm is sufficiently thick to protect the wafer surface through the etching of 1 μm SiO_2 and 20 μm Si device layer. Vertical etch of the patterns is achieved successfully using dry

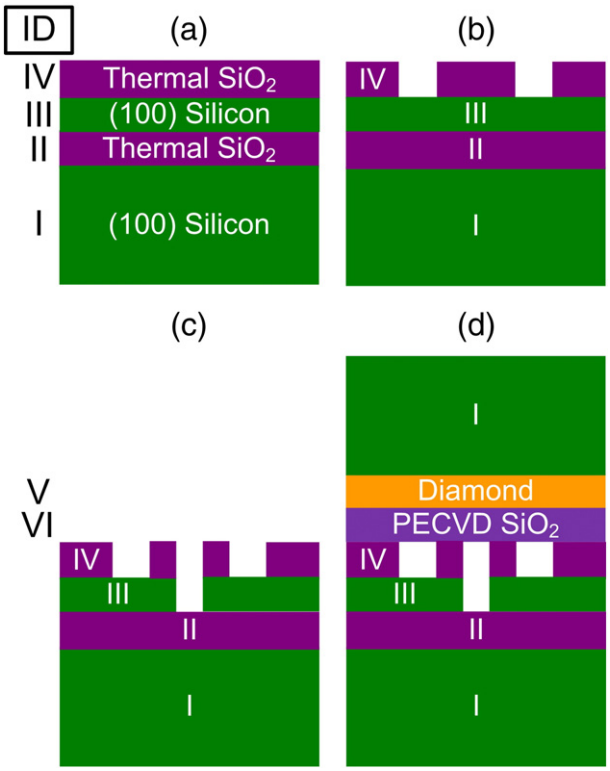

Fig. 1. Process steps used in the experiments. (a) SOI wafer with thermal SiO_2, (b) MASK1 patterning of cavity using RIE etch of SiO_2, (c) MASK2 patterning of separation between cavities using RIE etch of SiO_2 followed by DRIE etch of Si, and (d) direct wafer bonding of patterned wafer shown in (c) with a diamond-coated silicon wafer having PECVD SiO_2 on top.

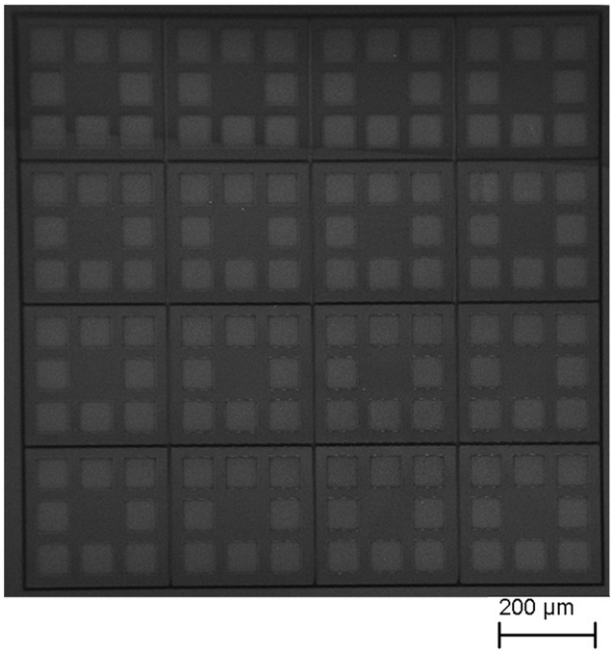

Fig. 2. Scanning electron microscopy (SEM) image of representative wafer similar to S_2 and S_4.